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Systems

IBM System/370 Model 115 Functional Characteristics

IBM

First Edition (March 1973)

Changes are periodically made to the information herein; before using this publication in connection with the operation of IBM systems, refer to the latest System Library Newsletter, *Accumulative Index of Publications and Programs – IBM System/360 and System/370,* GN20-0360, for the editions that are applicable and current.

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This publication describes the characteristics of the IBM System/370 Model 115, including the central processing unit, multiplexer channel, direct disk attachment, and the integrated attachments and adapters for other input/output devices. Its main purpose is to give systems analysts an understanding of the structure, features, and operations of the system. The manual also provides system programmers with information which is essential when writing and maintaining channel programs and operating systems for the System/370 Model 115.

In the six chapters of the manual, the characteristics of the Model 115 are described in terms of:

1. The basic system structure.
2. Main storage addressing.
3. The operations which can be performed and the means of manual and program control.
4. Compatibility features.
5. The commands, status and sense information for input/output devices attached other than through the multiplexer channel.
6. The characteristics of the integrated communications adapter.

Appendixes A, B, and C provide (respectively) code tables for the integrated communications adapter, instruction timings, and definitions of the abbreviations and special terms used in this manual.

The reader is assumed to be conversant with the IBM System/370 instruction sets, data formats, channel operations, and basic programming concepts such as status switching and interruption.

Prerequisite Reading

IBM System/370 System Summary, GA22-7001.
IBM System/370 Principles of Operation, GA22-7000.

Associated Publications

IBM System/370 Input/Output Configurator, GA22-7002.
General Information – Binary Synchronous Communications, GA27-3004.

The titles of other publications that may help the reader appear in *IBM System/360 and System/370 Bibliography,* GA22-6822 and its newsletter, *Accumulative Index of Publications and Programs,* GN20-0360.

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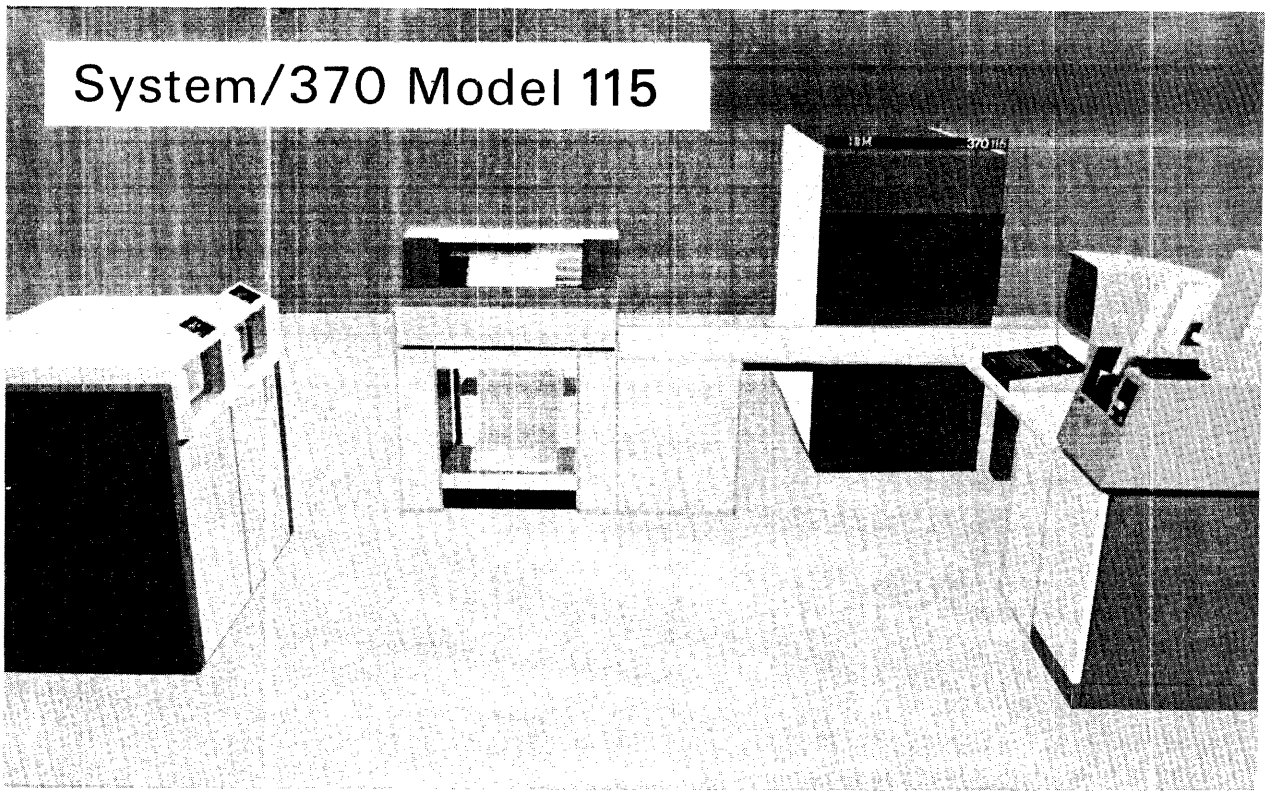
Note: The illustrations in this manual have a code number to the right of the caption. This is a publishing control number and is unrelated to the subject matter.

This chapter contains general information on the IBM System/370 Model 115. The following graphic pages show:

- The features of the system (Figures 1 and 2)
- The concept of the central processing unit (CPU) – the IBM 3115 Processing Unit (Figure 3)
- The system configuration (Figure 4)
- Simplified data flow (Figure 5).

The chapter closes with a short description of System/370 Model 115 operation.

A general-purpose data processing system of wide application – the low-cost entry into the System/370



Applications

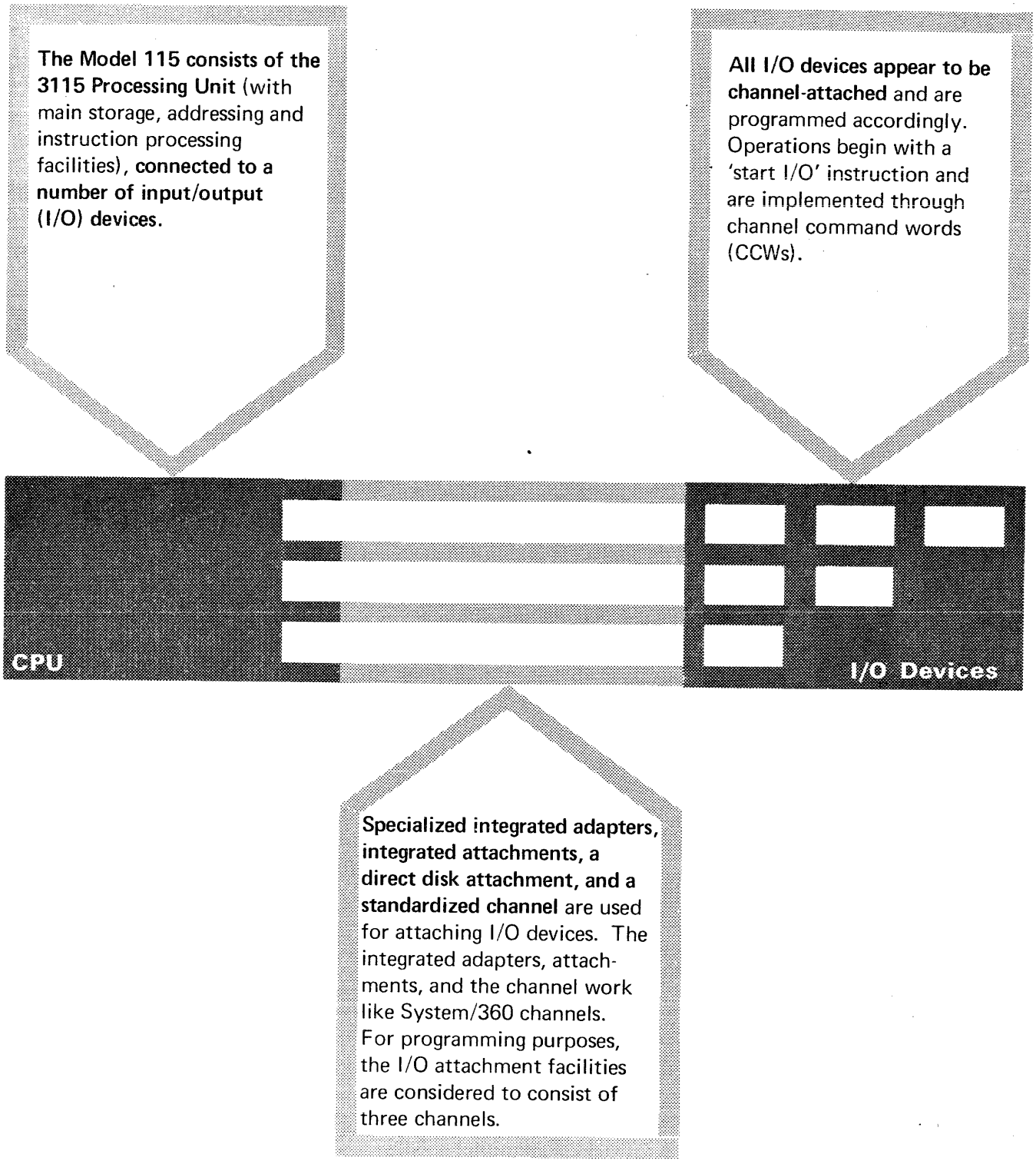
Commercial, scientific and teleprocessing

Compatibility

- Upward compatibility with IBM System/370
- Feature available for compatibility with IBM System/360 Model 20

System Profile

Figure 1. System Profile [10780]



System Features

Figure 2. System Features [10781]

Model 115 Design

The Model 115 has a decentralized design and consists of several independent subprocessors grouped round the main storage. A specialized unit therefore exists for each main system function, and there is little interference within the system.

The three types of subprocessors, located in the 3115 are:

- Machine Instruction Processor
- Service Processor
- Input/Output Processors.

Each subprocessor has its own storage, work registers, and an arithmetic and logic unit (ALU), and is controlled by its own micro-program and timing device.

B Machine Instruction Processor (MIP)

- Fetches and executes program instructions
- Carries out arithmetic/logical instructions entirely
- Analyzes I/O instructions so that the I/O processor can be selected
- Calculates addresses, sets condition codes, updates PSW
- Controls the direct disk attachment.

The MIP has a similar internal structure to that of an I/O processor, and uses a byte-wide data flow. To fulfill its tasks, the MIP includes special hardware such as:

A byte-sized shift unit
A six correction unit
An expanded local storage
An expanded control storage
A translation lookaside buffer with 8 associative arrays.

With these hardware and microprogram enhancements, the MIP is able to process more instructions than can be processed by an I/O processor, and can handle the full complement of System/370 instructions.

A Main Storage

- Nondestructive readout
- Storage cycle 480 nanoseconds (ns) per halfword
- Storage sizes (in bytes):
  65,536
  98,304

All storage has automatic correction of single bit errors in a halfword, and detection of double bit errors in a halfword.

Main Storage Controller

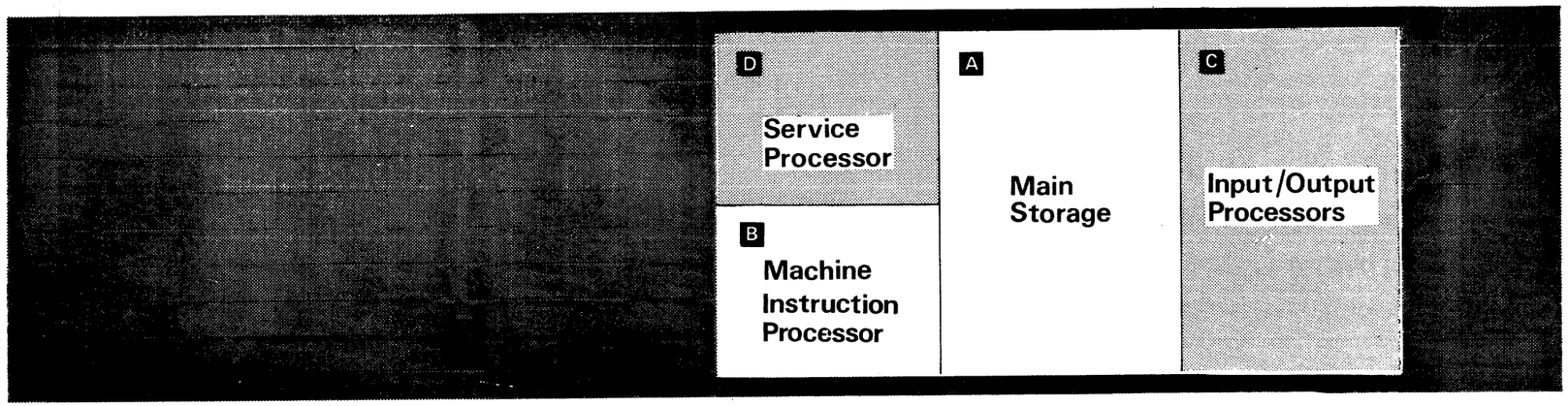
The main storage controller (MSC) regulates access to main storage. The MSC is composed of circuitry and has no microprogram. Subprocessors may request access at any time. At regular intervals the MSC examines requests and accepts the one with the highest priority, as follows:

HIGH PRIORITY	11 = Address stop
	10 = (Not used)
	9 = Multiplexer channel
	8 = Integrated communications adapter (ICA)
	7 = Direct disk attachment
	6 = (Not used)
	5 = Magnetic tape adapter
	4 = Integrated card input/output and printer attachments
	3, 2 = Spare
	1 = Service processor
LOW PRIORITY	0 = Machine instruction processor

Addressing

Main storage is addressed through address registers in the MSC local storage. Each subprocessor has two or more address registers (not available to the programmer). On a request from a subprocessor, the MSC uses the contents of the assigned register to address main storage. During access, the MSC updates the main storage address, and later returns it to the original local storage register. Thus, a subprocessor provides only the start address of the data field.

The MSC also notifies the requesting subprocessors of selection, data validity, and of errors such as protection violation, bad parity, and violation of the upper storage limit. Communication between the subprocessors and the MSC is over a data bus, a control bus, and direct control lines.



C Input/Output Processors (IOPs)

- Execute I/O commands
- Supervise data transfer between the addressed I/O device and MSC.

An IOP is a subprocessor with its own microprogram storage, ALU, internal and external work registers, and clock. It operates on a cycle of 450 nanoseconds. All IOPs have the same design. To meet the special needs of a connected I/O device, they are supplemented by a "front end" which is compatible with the I/O interface, over which signals pass to and from the device. Special microprograms are loaded to service attached I/O devices, and several microprograms can run concurrently in one IOP in "time-slicing" mode. Each identical IOP thus performs a different task, representing an attachment, adapter, or the multiplexer channel.

D Service Processor (SVP)

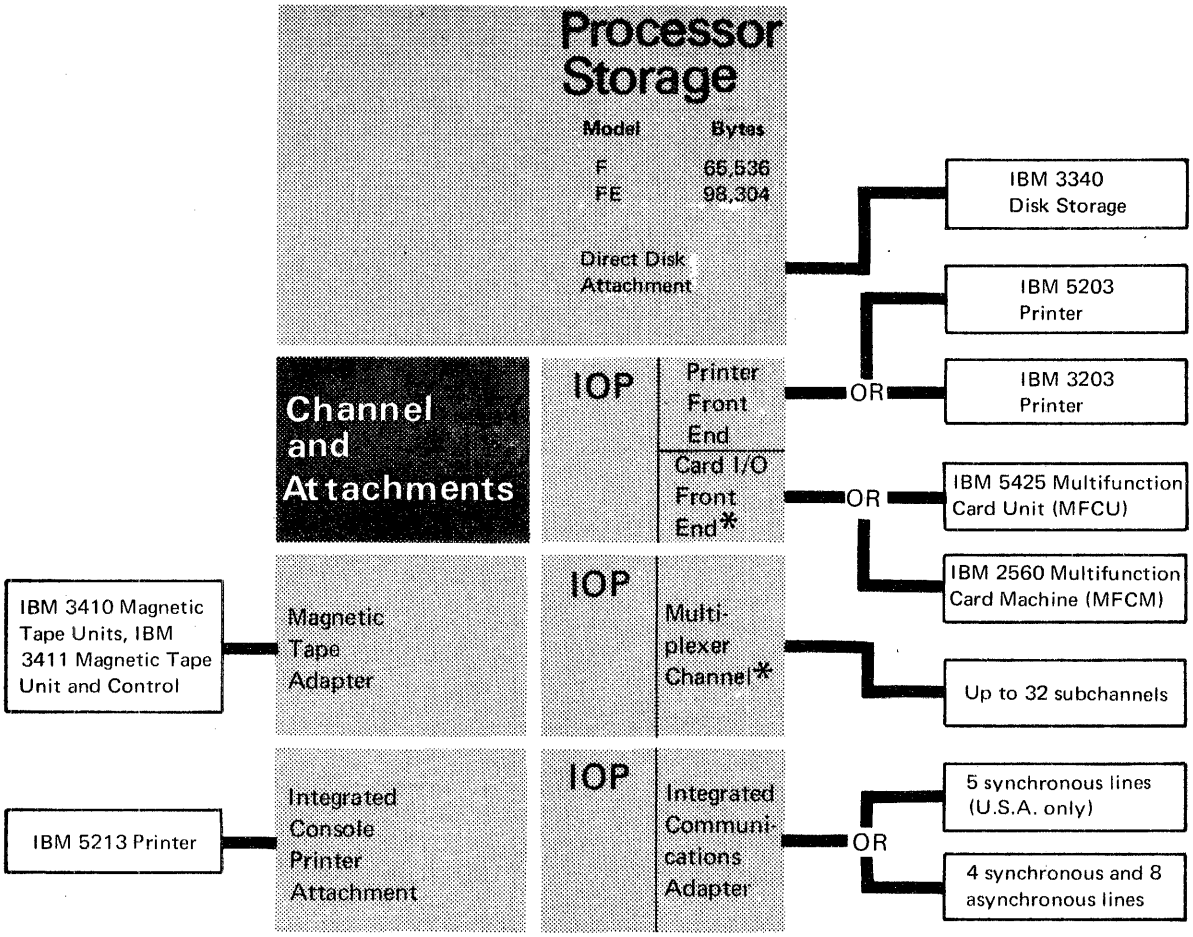
- Loads microprograms into all subprocessors (including itself)
- Provides the link between the operator and the system
- Reloads microprograms upon request from any IOP, logs error conditions and reads them out later for program analysis.

The SVP is a microprogram-controlled subprocessor with a data flow and ALU one byte wide. The small "bootstrap" program in read-only storage allows the SVP to load its own main microprogram from the console file. This file also stores the microprograms of the other subprocessors, and provides space for error logging.

The SVP contains local storage for handling data, and the circuitry for operating the console file and the operator console.

Figure 3. CPU Concept [10782]

CPU Concept



*Either the integrated card I/O attachment or the multiplexer channel, but not both, can be attached to the Model 115.

Features

Standard

Direct disk attachment
System/370 commercial instruction set
Byte-oriented operands
Store and fetch protection
Error correction and checking for main storage
Extended control mode
Dynamic address translation
Indirect data addressing
Program event recording
Monitor call
Location 80 timer
TOD clock, CPU timer, clock comparator
CPU and channel identification
Limited channel logout

Optional

External signals
Floating point instruction set
Byte multiplexer channel, or integrated attachment for a multifunction card I/O device
Integrated adapters for:
- Magnetic tape units
- Telecommunications

Integrated attachments for:
- Line printer
- Console printer

Feature for compatibility with System/360 Model 20

Configurator

Figure 4. Configurator [10783]

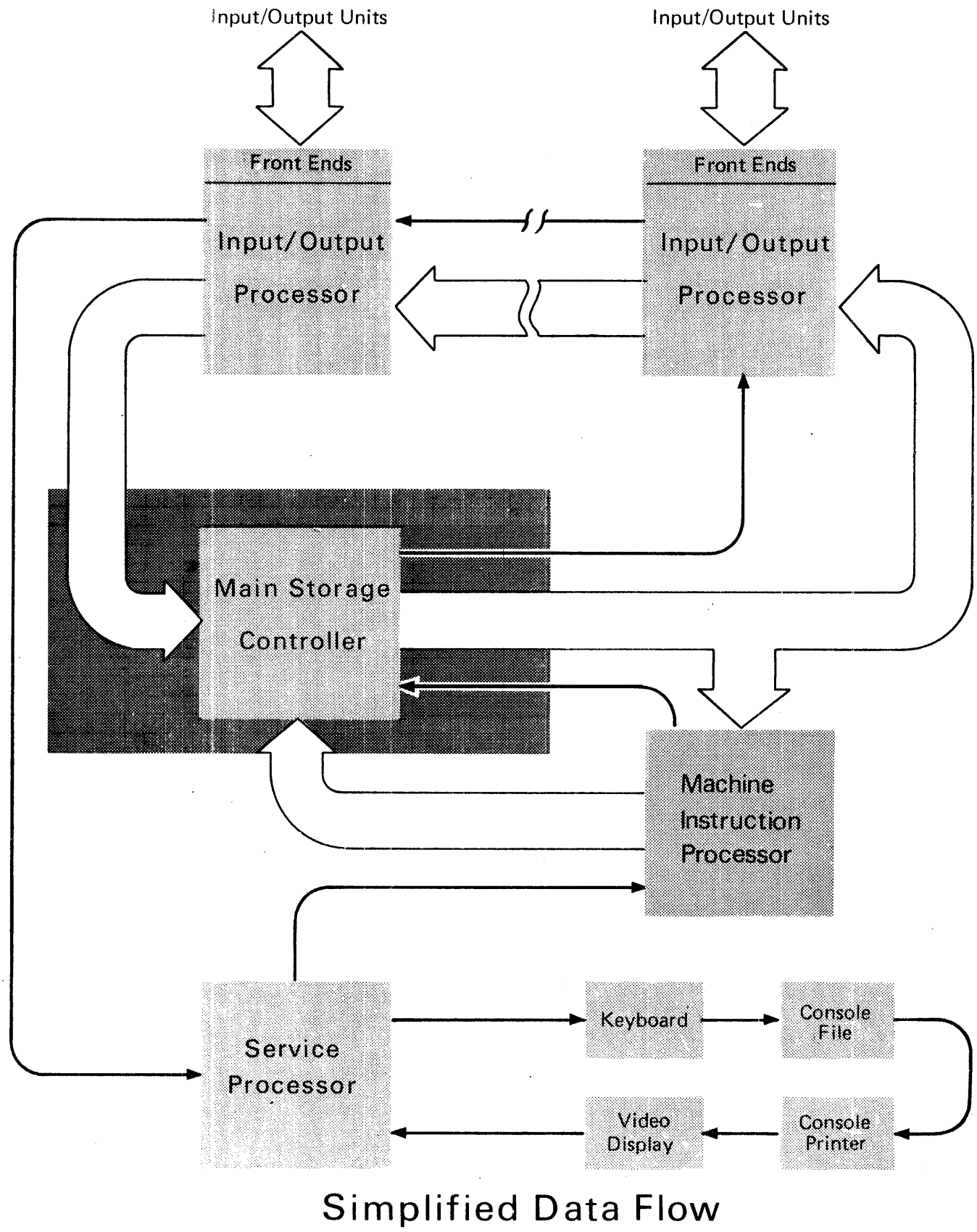


Figure 5. Simplified Data Flow [10784]

Outline of Operation

The Model 115 is generally under the control of an operating system. To prepare the system for operation, however, and also to check details and enter information, action must be taken by the operator.

OPERATOR CONSOLE

The operator controls the system by means of an operator console, which consists of a video display with a keyboard and control panel. The video screen displays the state of the machine in clear text. The keyboard allows the operator to display and alter registers and storage locations, or to enter new information.

POWER ON

To make the system operational, the operator must first press the POWER ON key. The key lights up red and remains red until the power-on sequence is completed, when it changes to white. The control storages of the various subprocessors are then automatically loaded, and corresponding messages such as 'MIP Loaded' appear on the screen. When loading is completed, the Model 115 is in manual mode and the operator can take over.

INITIAL PROGRAM LOADING

After the control storages have been loaded with microprogram, the program load display for the operator appears on the screen. Into this display, the operator keys the address of the device from which the program is to be entered. He must then make sure that the program medium (for example, magnetic tape or punched cards) is loaded into the device and that the device is ready. When he presses the ENTER key, loading begins and the screen is available to the operating system.

MACHINE OPERATION

As soon as the program is loaded, the machine takes over and the program is executed. From time to time, the operating system may send messages which are displayed on the video screen and/or printed out on the console printer (if installed). The operator may have to respond to these messages by keying in specifications.

Program Execution

Before the Model 115 executes a program, it must first analyze the current program status word. Depending on the setting of the PSW bits, interruptions will be allowed or disallowed, and certain modes will be set. The PSW also contains the address of the next instruction to be processed. This instruction is fetched by the machine instruction processor, which analyzes the operation code (op code) to find out which operation must be performed next.

Arithmetic and Logical Instructions

If the next instruction to be processed is arithmetic or logical, the MIP executes it (that is, a result is produced and placed in main storage, and a condition code showing the outcome is set). The program can use the condition code to branch to a specific routine.

I/O Instructions

If the next instruction to be executed is an input/output instruction, the MIP transfers it to the input/output processor responsible for the addressed I/O device. By means of a condition code, a response is sent through the IOP, allowing the program to branch, check on the actual condition (indicated in the CSW), or proceed normally.

The MIP waits only for the initial response, then fetches the next instruction. Thus the IOP is left to process the I/O command independently. In this way, the data transfer from or to main storage and the actions controlling the device are performed at the same time as logical operations in the MIP.

Interruptions

When an IOP has executed a command, it attempts to inform the program by requesting an interruption from the MIP. The MIP is prepared for such requests because, before executing each instruction, it checks whether interruptions are allowed. If they are allowed, the MIP scans for the interruption requests, and if the interruption request line (from all IOPs to the MIP) is active, it does not execute the next sequential instruction, but switches instead to a new PSW.

By introducing a new PSW, the MIP has also brought in a new address for the next sequential instruction. Consequently, the MIP fetches an instruction from a different storage location owing to the switching of the PSWs, and the interruption has the effect of a program branch.

The program branch is usually to a routine which examines the interruption code in the old PSW to determine the interruption source. If the source was, for example, an I/O device which had finished delivering data to main storage, the program will now process this data. When the processing is completed, the program will restore the old PSW as the current PSW, thus continuing at the point of interruption.

Manual Operations

Manual operations are those performed by the operator and not by the program. First, the operator brings the mode selection display onto the video screen by pressing the

MODE SEL (mode selection) key. The 3115 Processing Unit does not stop, but the screen is now no longer available for messages from the operating system.

The mode selection display (Figure 6) shows the repertoire of modes (with selector characters) which are available to the operator. The operator selects a mode by keying in the selector character at the keyboard and pressing the ENTER key.

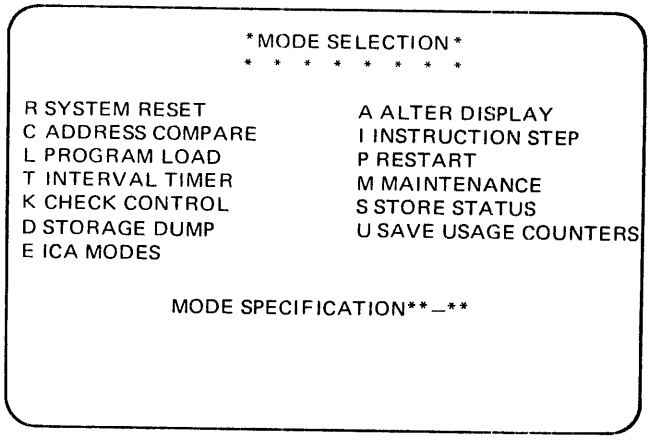


Figure 6. Video Display – Mode Selection [10785]

The following paragraphs describe, as examples, the actions the operator must take to select and to perform operations in two typical modes. For further information, see the description of mode selection in the "Operator Controls" section of "System Control".

Program Load

If the manual operation to be performed is program load, the operator must select 'L' (by pressing 'L' on the keyboard) and then press the ENTER key. The program load display (Figure 7) will then appear on the screen. The operator enters the address of the device from which the program is to be loaded by means of the alphameric keys, and the selected address appears in hexadecimal characters on the screen under 'Channel', 'Control Unit', and 'Device'.

Program loading begins with a system reset which the operator can specify as "normal" or "clear" by keying in 'N' or 'C'. In normal loading, the general registers, floating point registers, control registers, and main storage contents remain unchanged but the parity is made valid in all registers. In clear loading, these facilities are reset to zero (with valid parity), except the control registers, which are initialized.

Providing no errors have been made and the selected device is loaded and ready, pressing the ENTER key will now cause program loading to commence.

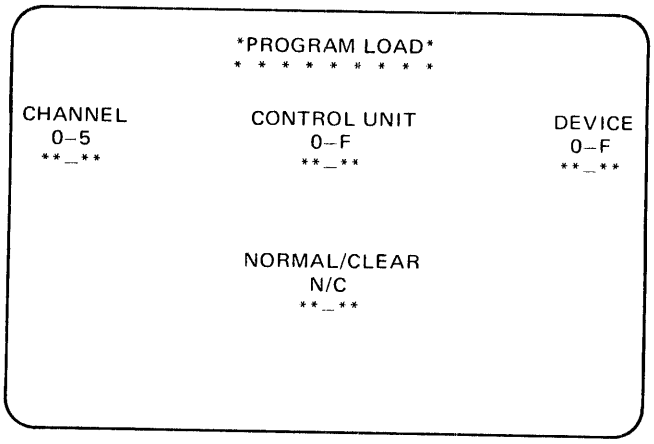


Figure 7. Video Display – Program Load [10786]

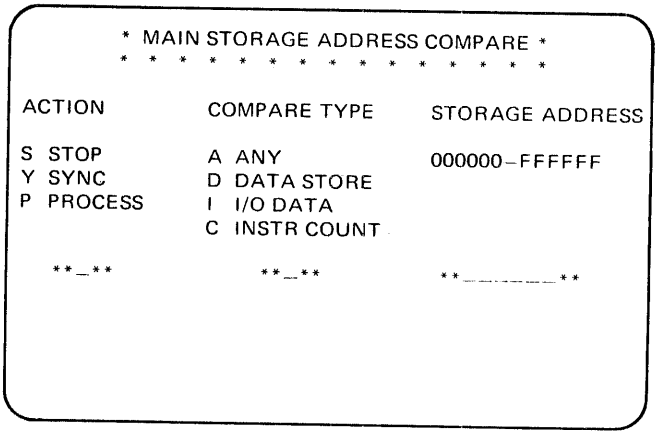


Figure 8. Video Display – Main Storage Address Compare [10787]

Address Compare

If the operator wishes to perform an address compare operation, he must first key 'C' into the mode selection display and then press ENTER. The main storage address compare display (Figure 8) will appear on the screen.

Under 'Storage Address', the operator keys in the main storage address which is the subject of the address compare operation (the search address). Under the 'Compare Type' heading, the operator keys in a code letter which represents one of four possible types of compare operation.

1. *Any (A).* If the operator keys in code 'A', all addresses used in the system are checked against the search address.
2. *Data Store (D).* If the operator keys in code 'D', only addresses used by the CPU to store data into main storage are compared with the search address.
3. *I/O Data (I).* If the operator keys in code 'I', only addresses used in transferring data to and from input/output devices are compared with the search address.

4. *Instr Count (C).* If the operator keys in code 'C', only addresses used by the CPU to fetch instructions (instruction count) are compared with the search address.

Under the 'Action' heading, the operator keys in a code letter which represents the action the machine should take when an address match occurs. If the operator keys in code 'S' (stop), the machine halts as if the STOP key had been pressed. If code 'Y' (sync) is keyed in, a signal is made available for the customer engineer. If code 'P' (process) is keyed in, address compare mode is turned off, and the Model 115 is restored to normal processing.

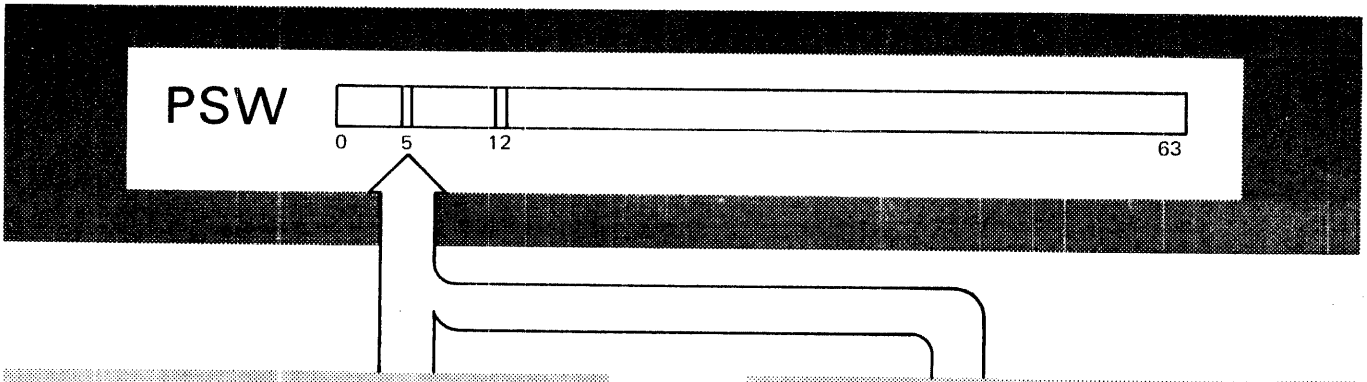
In the System/370 the addressable main storage is not confined to the storage bytes physically installed in the CPU. These bytes of "real storage" are supplemented by a large area of "virtual storage" on an external file. By this arrangement programmers can address up to 16,777,217 bytes of storage, even though, for example, only 65,536 bytes may be installed in the CPU.

When bytes of virtual storage are addressed by the program they are automatically called into main storage on a "page" of information, and their addresses are adjusted by a translation process.

The virtual storage facility is supported by three standard features: dynamic address translation, extended control mode, and indirect data addressing.

This chapter consists of five graphic pages on main storage addressing. The first graphic page shows how either normal address computation or dynamic address translation may be specified (Figure 9). The remaining pages show how, in the process of dynamic address translation, virtual addresses are converted to real addresses in three successive steps (Figures 10 to 13).

To obtain access to main storage, the MIP must place a real address, which falls within the main storage boundaries, into MSC local storage. The method of address generation is determined by PSW bit 5.



0=Normal Address Computation

If PSW bit 5 is off, the MIP computes addresses by adding the 12-bit binary displacement to the 24-bit base address. In RX instructions, the 24-bit index is also added. Since overflows are ignored, the result is always a 24-bit binary number representing a real address within the main storage limits.

The MIP transfers the 24-bit number to the MSC, without change, in two steps. First, the sixteen low-order address bits are loaded, then the two high-order bits and the four-bit protection key. During step two, the MSC checks if the storage boundary has been surpassed, and if so, sets a check bit, which later causes an addressing error indication when the address is used.

1=Dynamic Address Translation

If PSW bit 5 is set, the MIP forms a 24-bit address in the same way as when the bit is off, but does not take this as a real address within the main storage limits. Instead, the 24-bit binary number is interpreted as a virtual address and the steps described in Figures 11 to 13 are carried out. Setting PSW bit 5 for dynamic address translation is only effective when PSW bit 12 has also been set to place the Model 115 into EC mode.

Types of Main Storage Addressing

Figure 9. Types of Main Storage Addressing [10788]

The virtual address shown below consists of the segment address, the page address, and the byte address.

The segment address is added to the segment table origin address located in bits 8 to 25 of control register 1. The resulting binary number points to a specific entry of the segment table in main storage.

Using the computed binary number as a real address, the MIP fetches the contents of the selected segment table entry and adds them to the page address portion of the 24-bit virtual address. The resulting binary number points to an entry in the page table.

The contents of the selected page table entry represent the high-order part of the real address. The byte address portion of the virtual address is attached as the low-order part, and the resulting bit string represents the real address.

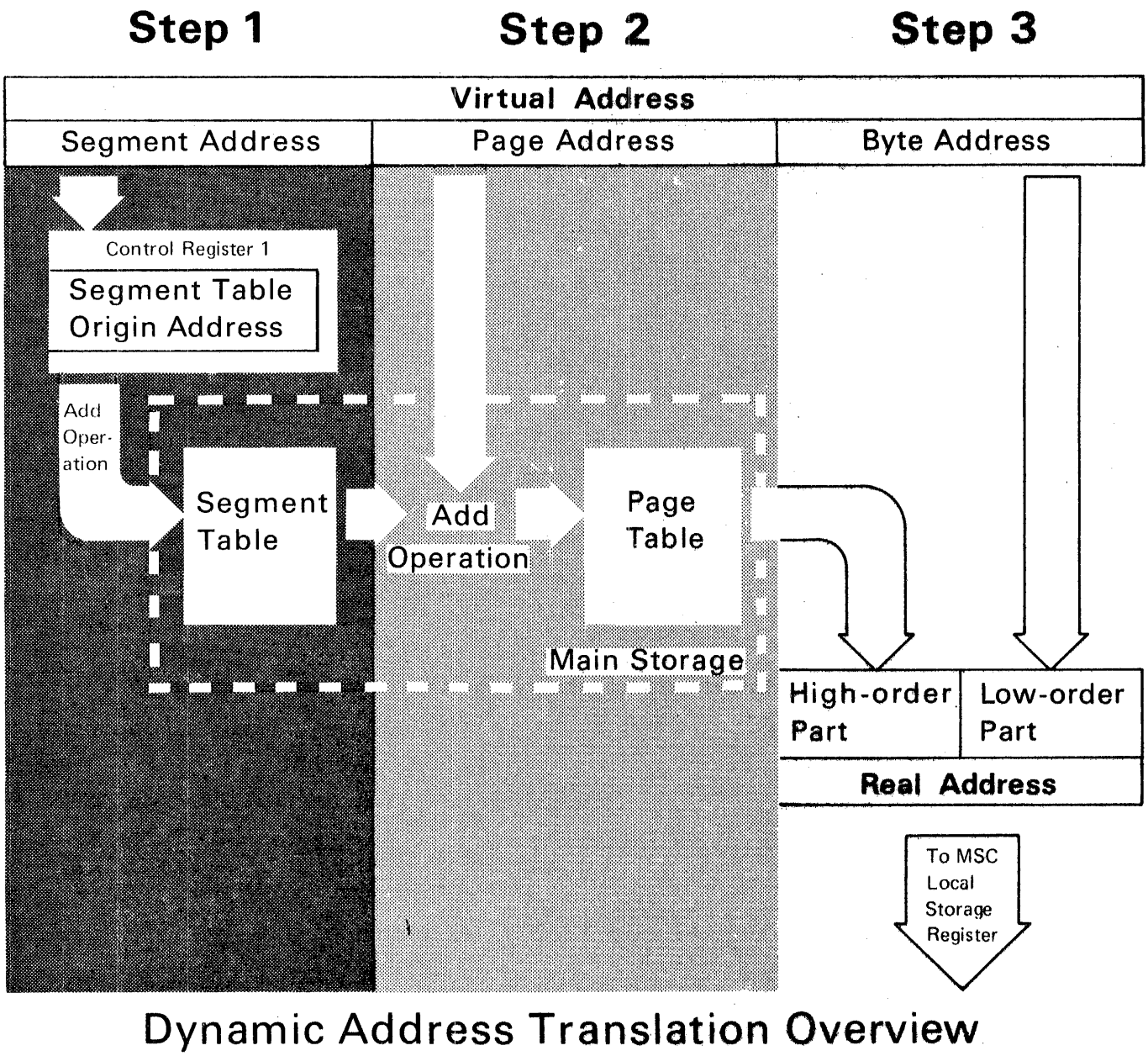


Figure 10. Dynamic Address Translation Overview [10789]

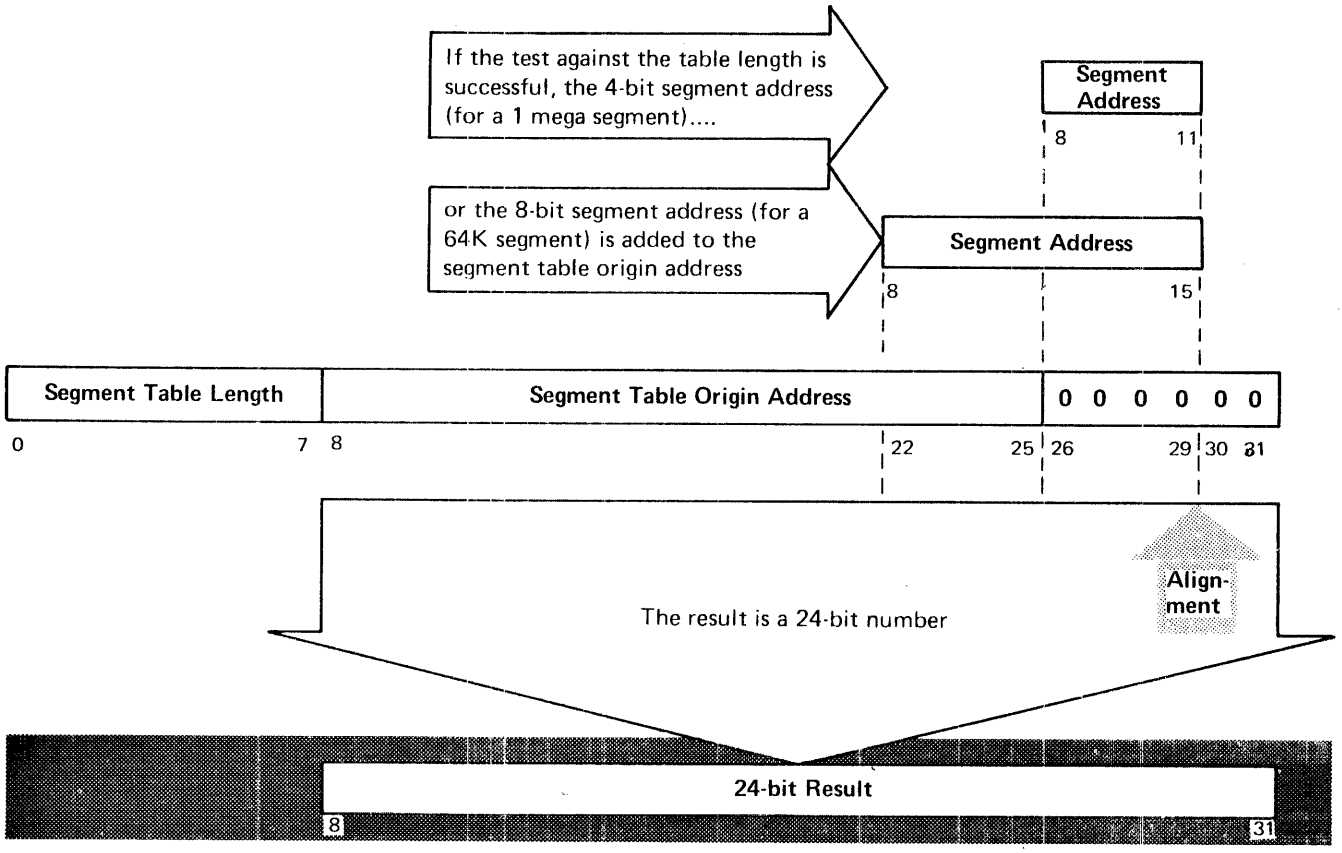
Tests

1 Mega Size

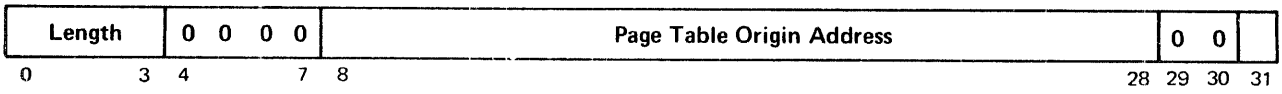
A string of eight zero bits is generated and compared with the segment table length specification in bits 0 to 7 of control register 1. (Zeros are used because bits 1 to 7 do not exist in a 24-bit virtual address.) A segment translation exception is indicated if the virtual address bits represent a value larger than the length specification.

64K Size

The segment table length specification in control register 1 is extended with three high-order zeros and compared with bits 1 to 11 of the virtual address. Because only bits 8 to 11 exist in a 24-bit address, bits 0 to 7 are generated as zeros to allow for comparison. If the test shows that the 24-bit result address will designate an entry within the segment table, the add operation is performed, and the entry is fetched from main storage; if not, a segment translation exception is indicated. The segment table must be located in real storage.



The data fetched from the segment table is a 32-bit field containing information which allows access to the page table:

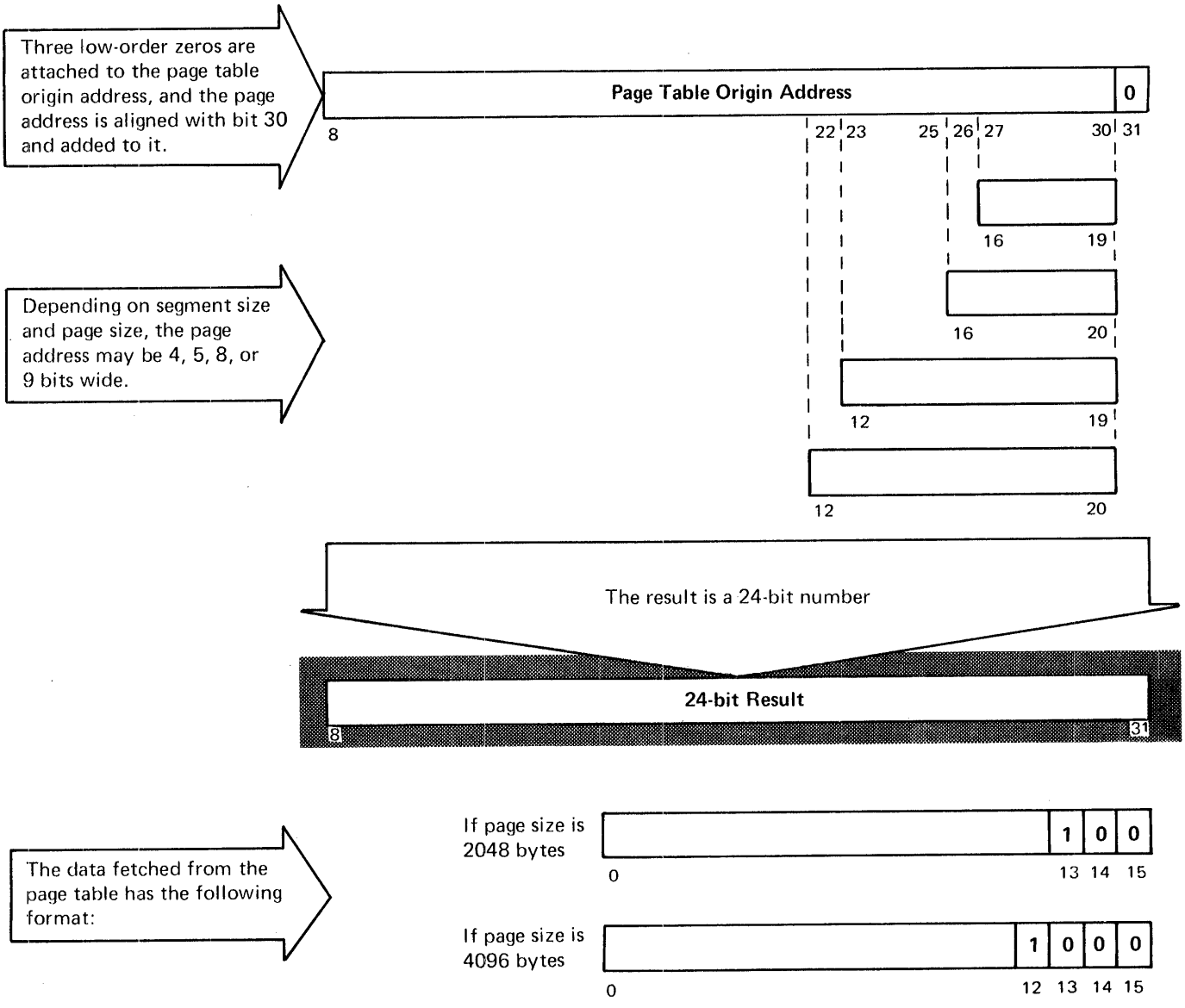


Dynamic Address Translation Step 1

Figure 11. Dynamic Address Translation Step 1 [10790]

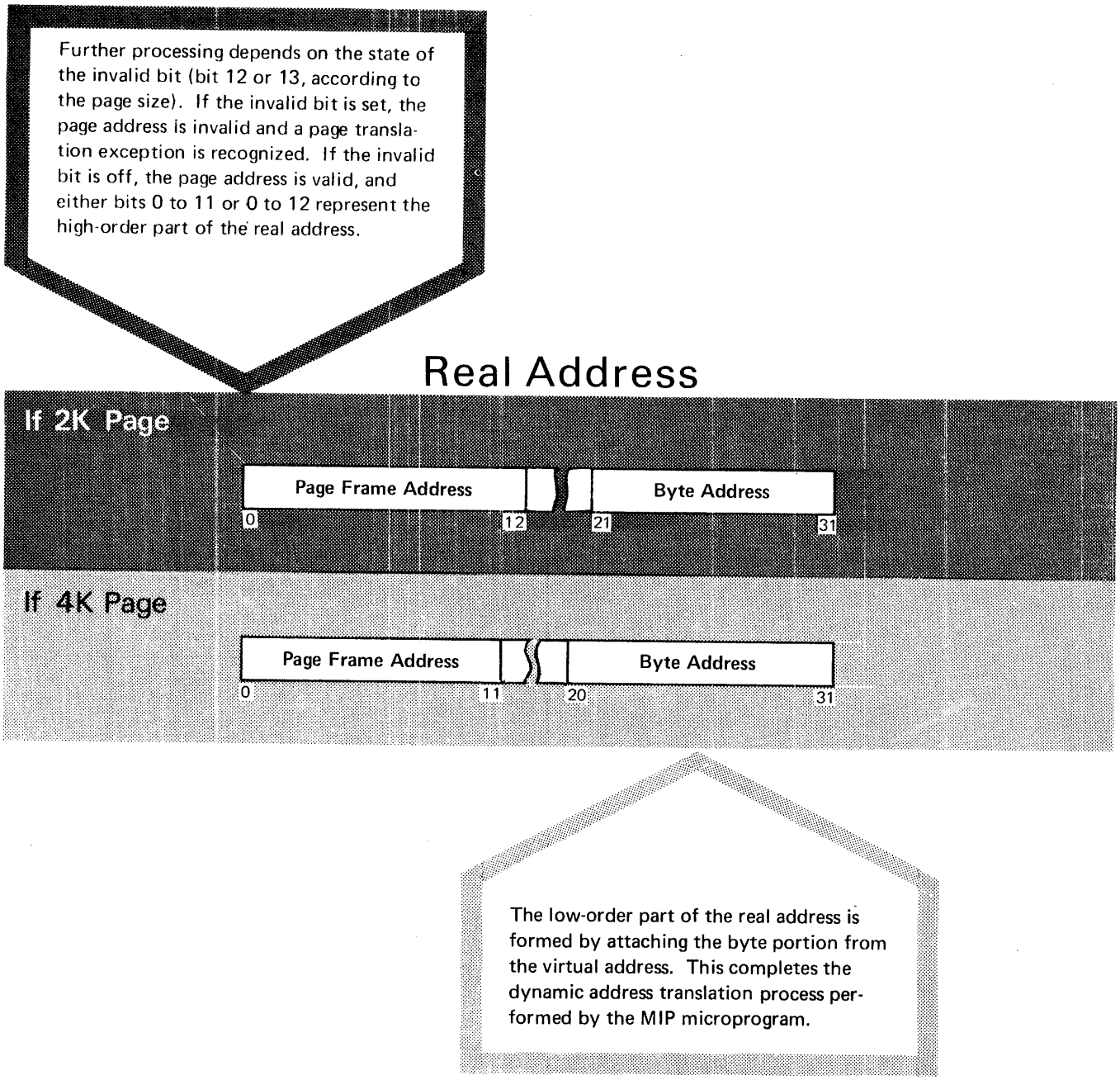
As a prerequisite for translation step 2, the invalid bit (bit 31) in the segment table entry must be zero. A one-bit causes a segment translation exception.

A length check is carried out to ensure that the computed page table address points to an existing page table entry. In this check, the four high-order bits of the page address are compared with the length code (bits 0 to 3) of the data fetched from the segment table. If the length code is smaller, a page translation exception is recognized. If the check is satisfactory, the 24-bit address is used to fetch the selected page table entry.



Dynamic Address Translation Step 2

Figure 12. Dynamic Address Translation Step 2 [10791]



Dynamic Address Translation Step 3

Figure 13. Dynamic Address Translation Step 3 [10792]

The Model 115 is controlled by means of the following main facilities:

- **Program status words**
- **Control registers**
- **Fixed areas in main storage**
- **Interruption mechanism**
- **Timers**
- **Operator console**

All of these control facilities are available to the operating system and/or the operator.

Program Status Words

The PSW is the most important factor in system control, because it contains the basic information required for running programs. Throughout the course of a program, the PSW provides the internal control mechanism with information on where the next instruction is located, which facilities are masked off, and which states and modes apply. The PSW is a doubleword (that is, 64 bits long) with a choice of two formats. The format is determined by the state of PSW bit 12: when this bit is off, it specifies basic control mode, when set, it specifies extended control mode. The microprogram always examines bit 12 first because it determines how the rest of the PSW is to be interpreted.
Note: In System/360 machines, PSW bit 12 specifies either EBCDIC or ASCII mode. This choice is not available in the Model 115, which always uses EBCDIC as its internal code.

PSW IN BC MODE

A PSW in which bit 12 is off is interpreted as shown in Figure 14. The PSW bit assignment in BC mode is similar, but not identical, to the format in System/360. For instance, when the external mask bit (PSW bit 7) is set, it is only effective in BC mode for those interruption-requesting sources which have a subclass mask bit set in control register 0 (see Figure 18).

Loading a BC Mode PSW

When a BC mode PSW is set up by means of the 'load PSW' instruction, the doubleword designated by the operand address is loaded as the current PSW. The interrupt code (bits 16–31) and the instruction length count (bits 32–33) of the current PSW loaded in this way are always zero.

Changing Bits in the BC Mode PSW

Several instructions are available to the programmer for changing PSW bits. New information can be placed into PSW bits 0 to 7 by means of the 'set system mask' instruction, or individual bits can be changed by the instructions 'store then OR system mask' and 'store then AND system mask'. The program mask (PSW bits 36 to 39) can be replaced with a new mask by giving the 'set program mask' instruction, which also introduces a new condition code. The instruction address (PSW bits 40 to 63) can be changed by means of the 'branch and link' instruction.

BC Mode PSW Errors

If a PSW containing any of the following errors is introduced by a 'load PSW' instruction or by an interruption, these errors will be recognized during the execution of the next instruction:

- A one-bit, pointing to an odd boundary, is in the low-order position (PSW bit 63) of the instruction address (specification error).
- The location specified by the instruction address is outside the available main storage (addressing error).
- The location specified by the instruction address is protected against fetching (protection error).

The detection of any of these errors causes a specification exception interruption during which the invalid PSW is stored as the old PSW, the instruction length count having a value of 1, 2, or 3 to indicate the number of halfwords by which the instruction address has been updated. The extent of this updating (1, 2, or 3 halfwords) depends on the format of the instruction (RR, RX/RS/SI, or SS) in progress when the exception is recognized.

There are conditions in which the invalid PSW may not be recognized. If the invalid PSW enabled pending I/O and/or external and/or machine check interruptions, these interruptions would occur instead of any interruptions caused by the errors listed above, thus preventing recognition of the invalid PSW. The same applies if the invalid PSW has the wait state bit set, because the CPU then enters the wait state and leaves it only through an interruption, which again prevents detection of the invalidity.

0—5 Channel Mask

Bits 0 to 5 are assigned to channels 0 to 5. When a channel mask bit is set, I/O interruptions are enabled for the respective channel. If a bit is off (zero), interruptions are disabled for that channel. The interruption conditions remain pending.

6 Input/Output Mask

1 = Interruptions are enabled for channel 6 and above.
0 = Interruptions are disabled for channel 6 and above.
These channels are not available on the Model 115.

7 External Mask

1 = Interruptions are enabled from the following external sources:
- Location 80 timer
- CPU timer
- Clock comparator
- Interrupt key on console
- External signals

0 = External interruptions are disabled.
Note: CPU timer and clock comparator interruption conditions remain pending only if no new values are set before the interruption is taken.

8—11 Key

This is a binary key which is compared with a key in storage when the CPU stores a result or fetches data from a fetch-protected location. Fetching and storing only succeed if these two keys match or the PSW key is zero.

12 Extended Control Mode

1 = EC mode is set and the PSW bits are interpreted as shown in Figure 15.
0 = Basic control (BC) mode is set and the PSW bits are interpreted as shown in this Figure.

13 Machine Check Mask

1 = Interruptions due to machine checks (such as parity errors, system, processing, or timer damage) are enabled.
0 = Interruptions due to machine checks are disabled. They remain pending.

14 Wait State

1 = The CPU is in the wait state (no instruction processing by MIP and no CPU meter recording).
0 = The CPU is in the running state.

15 Problem State

1 = The CPU is in the problem state, and only unprivileged instructions are executed.
0 = The CPU is in the supervisor state, and both privileged and unprivileged instructions are executed.

16—31 Interruption Code

This is a binary code which identifies the source of an interruption.

32—33 Instruction Length Code

This is a binary code which shows the length of the last-interpreted instruction (1, 2, or 3 halfwords) when a program or supervisor call interruption occurs.

34—35 Condition Code

This is a binary number set by the results of various instructions, so that branching decisions can be made.

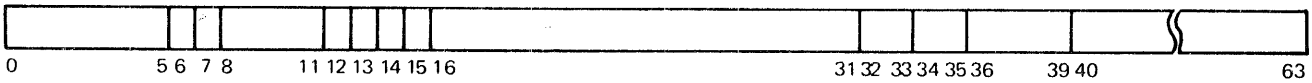
36—39 Program Mask

When set the program mask bits enable interruptions due to:
- Fixed point overflow (bit 36)
- Decimal overflow (bit 37)
- Exponent underflow (bit 38)
- Significance (bit 39)

If the bits are 0, the relevant interruptions are disabled.

40—63 Instruction Address

This is a binary field representing the main storage address of the next instruction to be executed.



Program Status Word (BC Mode)

Figure 14. Program Status Word (BC Mode) [10793]

PSW IN EC MODE

When bit 12 of the current PSW is set, the contents of the PSW are interpreted as shown in Figure 15. Some of the bit assignments are the same as in the BC mode PSW. Bits 8 to 11, 13, 14, and 15, for instance, are identical in meaning for both BC mode and EC mode PSWs. Other assignments differ. For example, the BC mode PSW contains an instruction length count and an interruption code, but when EC mode is specified, these two fields are located in a fixed area of main storage.

Loading an EC Mode PSW

When an EC mode PSW is set up by means of the 'load PSW' instruction, the doubleword designated by the operand address is loaded as the current PSW. In contrast to the BC mode PSW, the EC mode PSW is loaded unchanged, and none of the bits is forced to zero. The reason is that in EC mode the instruction length count and interruption code are located in fixed areas of main storage and not in the PSW.

Changing Bits in the EC Mode PSW

Several instructions are available to the programmer for changing PSW bits. New information can be placed into PSW bits 0 to 7 by means of the 'set system mask' instruction, or individual bits can be changed by the instructions 'store then AND system mask' and 'store then OR system mask'. The program mask (PSW bits 20 to 23) can be replaced by means of the 'set program mask' instruction. The instruction address (PSW bits 40 to 63) can be changed by means of the 'branch and link' instruction.

EC Mode PSW Errors

When an EC mode PSW containing errors is introduced by a 'load PSW' instruction or by an interruption, certain errors are recognized while the next instruction is being executed, and other errors are recognized immediately. The following error causes a specification exception interruption before the PSW becomes active:

- One or more unassigned bits are set. (Bits 0, 2, 3, 4, 16, 17, and 24 to 39 are unassigned and must be zero.)

Should this error be detected, a specification exception interruption occurs, even if the invalid PSW enables pending I/O or machine check interruptions, or has the wait state bit set. The specification exception interruption thus takes priority. The pending I/O or machine check interruptions are under the control of the new PSW introduced by the specification exception interruption. The wait state bit is ignored when the described error occurs.

The specification exception interruption, which occurs immediately when the error is detected, causes the instruction length count (in main storage) to be reset to zero because instruction processing has not been started.

The following errors in an EC mode PSW are recognized during the execution of the next instruction:

1. The low-order bit of the instruction address (PSW bit 63) is set (that is, an odd address is specified).
2. The location designated by the instruction address is outside addressable storage, or is protected against fetching.

If either of these errors is detected, an interruption occurs. The instruction length count in main storage is updated by one, two, or three, indicating the number of halfwords by which the instruction address was updated. The updating depends on the format of the instruction in progress when the exception is recognized. Any pending I/O interruptions or machine check interruptions enabled by the invalid PSW will, however, occur, and the invalidity of the PSW is therefore not detected. The same applies when the invalid PSW has the wait state bit set, because the CPU then enters the wait state and leaves it only by an interruption which again prevents detection of the PSW invalidity.

1 Program Event Recording Mask

1 = Program events specified in control register 9 (such as successful branching) will cause an interruption.
0 = Program event recording is disabled.

5 Translation Mode

1 = Dynamic address translation is used (the address base + displacement is translated via segment and page tables into the real storage address).
0 = Address translation is not used.

6 Input/Output Mask

1 = I/O interruptions are enabled for all channels whose mask bits in control register 2 are set.
0 = All I/O interruptions are disabled, and requests remain pending.

7 External Mask

1 = External interruptions are enabled for all sources whose mask bits in control register 0 are set.
0 = External interruptions are disabled.

8–11 Key

This is a binary key which is compared with a key in storage when the CPU stores a result or fetches data from a fetch-protected location. Fetching and storing only succeed if the keys match or the PSW key is zero.

12 Extended Control Mode

1 = Model 115 is in EC mode and the PSW bits are interpreted as shown in this Figure.
0 = Model 115 is in BC mode and the PSW bits are interpreted as shown in Figure 14.

13 Machine Check Mask

1 = Machine check interruptions are enabled for:
- System and processing damage.
- All other machine checks whose mask bits in control register 14 are set.

0 = Machine check interruptions are disabled.

14 Wait State

1 = The CPU is in the wait state (no instruction processing by MIP and no CPU meter recording).
0 = The CPU is in the running state.

15 Problem State

1 = The CPU is in the problem state, and only privileged instructions are executed.
0 = The CPU is in the supervisor state, and both privileged and unprivileged instructions are executed.

18,19 Condition Code

This is a binary number set by the results of various instructions, so that branching decisions can be made.

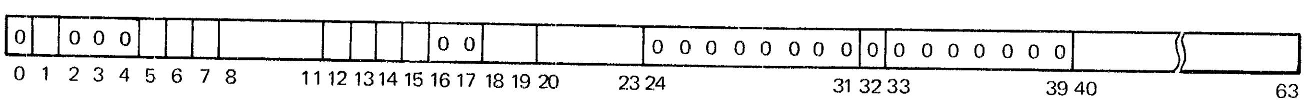
20–23 Program Mask

When set, these bits enable interruptions due to:
- Fixed point overflow (bit 20)
- Decimal overflow (bit 21)
- Exponent underflow (bit 22)
- Significance (bit 23)

If a bit is 0, relevant interruption is disabled (the condition remains pending).

40–63 Instruction Address

This is a binary field representing the main storage address of the next instruction to be executed.



Program Status Word (EC Mode)

Figure 15. Program Status Word (EC Mode) [10794]

Control Registers

The control registers (Figures 16 to 23) are a standard feature on the Model 115. The feature provides 16 registers, each of which is one word (32 bits) wide. The registers are not part of addressable main storage, they are located in the MIP. The bits in these registers define how certain features such as monitoring, program event recording, and dynamic address translation are to operate.

The control registers are automatically initialized during a system reset operation, but they can also be loaded by means of the 'load control' instruction. This instruction contains two register specification fields, the first of which defines the first register to be loaded, the other defines the last register to be loaded. The operand address designates the storage location from which the data is to be fetched. During execution, the instruction causes as many words to be fetched from main storage (in ascending order of address) as are required to fill the number of control registers specified (including the first and the last).

The contents of the control registers can be made available for inspection by means of the 'store control' instruction. This instruction causes the opposite effect of the 'load control' instruction, that is, the contents of as many registers as are specified are placed in main storage.
Note: The first register to be loaded or stored may be any of the 16 registers, it need not be register 0. The count wraps around during loading or storing and continues in ascending order until the last register is reached. The last register may, likewise, be any of the 16 registers.

The following is supplementary information related to individual control registers.

BLOCK MULTIPLEXING CONTROL

When bit 0 of Control Register 0 (see Figure 18) is set, disk files operate in block multiplexing mode and interleaving is allowed. For example, if command chaining has been specified and channel end is presented separately from device end, the channel logically disconnects from the control unit to make the interface available for other disk operations. In block multiplexing mode, the channel also provides a 'channel available' interruption to indicate to an instruction which previously caused a channel busy response (condition code 2) that it may now proceed.

MONITORING

Control register 8 (see Figure 20) contains the monitor mask bits for the Monitoring feature which is standard in the Model 115. Monitoring provides the means to record and analyze software events such as entry or exit from specific subroutines, program execution time, and the sequence in which programs were entered.

Each bit in the monitor mask field (bits 16 to 31 of control register 8) represents a class of events, and the bit setting determines whether or not the class is to be monitored. Each bit can be addressed by a 'monitor call' instruction.

The 'monitor call' instruction contains a monitor class number that can range from 0 to 15. The number 0 addresses mask bit 16, number 1 addresses mask bit 17, number 2 addresses mask bit 18, and so on. When the 'monitor call' instruction addresses a mask bit that is 0, the instruction has no effect (no-op). However, when the 'monitor call' instruction addresses a mask bit that is set, an interruption occurs.

The interruption causes the class number (in the instruction), the result of the B1/D1 field of the instruction (the monitor code), and a monitor interruption bit to be stored in main storage. Class number, monitor code, and monitor interruption bit together identify the cause of the interruption and the unique monitoring event that is thus indicated. A program can be monitored in detail by including 'monitor call' instructions at strategic points.

PROGRAM EVENT RECORDING

Program event recording (PER), which is a standard feature of the Model 115 but available in EC mode only, is handled through control register 9 (see Figure 21). Bits 0 to 3 and 16 to 31 specify which predefined event (such as a successful branch, instruction fetching, or storage alteration) can cause an interruption. Bits 4 to 15 are not assigned.

When a particular bit is set, the assigned event is monitored and an interruption is requested when the event occurs. Whether or not the interruption takes place depends on the PER mask bit in the EC mode PSW (bit 1). The interruption can only occur if PSW bit 1 is set. The cause of the interruption is identified as described in the following text.

Successful Branch

When bit 0 of control register 9 is set, the instructions 'branch on condition', 'branch and link', 'branch on count', 'branch on index high', and 'branch on index low or equal' are being monitored. If one of these instructions causes a branch, the address to which the instruction branched is placed into the program old PSW, and the address of the instruction that caused the branch is placed into the program event address field of main storage during the interruption. If the successful branch instruction is the object of an 'execute' instruction, the address of the 'execute' instruction is recorded in main storage.

Instruction Fetching

When bit 1 of control register 9 is set, the main storage area defined by the start and end addresses in control registers 10 and 11 is monitored. If an instruction which has its first (leftmost) byte in this area is fetched, the event occurs. During the resulting interruption, the updated instruction address is transferred to the program old PSW, and the address of the first byte of the instruction is recorded in the program event address field in main storage. In addition, the instruction length code is set to indicate the length of the instruction that caused the event. If the instruction is the object of an 'execute' instruction, the address of the 'execute' instruction is recorded.

Storage Alteration

When bit 2 of control register 9 is set, the storage area defined by the start and end addresses in control registers 10 and 11 is monitored for alteration. The monitoring is limited to operations in which the MIP replaces part or all of an operand. Typically, these are operations such as move, shift, edit, and arithmetic operations. An operand is considered to have been altered even if it has merely been shifted by zero, or if a zero has been added.

Automatic CPU operations such as timer updating, PSW exchange during interruption, and so on (that is, operations not caused by an explicit instruction) are not monitored. If the timer value is changed by an instruction, however, a program event is recognized.

When main storage is altered within the monitored area, the resulting interruption causes the address of the instruction responsible for the alteration to be recorded in the event address field in main storage, and the updated instruction address is placed in the program old PSW. If the altering instruction is the object of an 'execute' instruction, the address of this 'execute' instruction is recorded.

General Register Alteration

When bit 3 of control register 9 is set, bits 16 to 31 determine which general register is being monitored. If bit 3 is zero, alterations to the general registers cannot cause interruptions.

Bits 16 to 31 of register 9 correspond to the general registers 0 to 15. If any of these bits is set, the assigned general register is monitored for alteration. If the monitored register is altered, an interruption can occur only if bit 3 in control register 9 and PSW bit 1 are set.

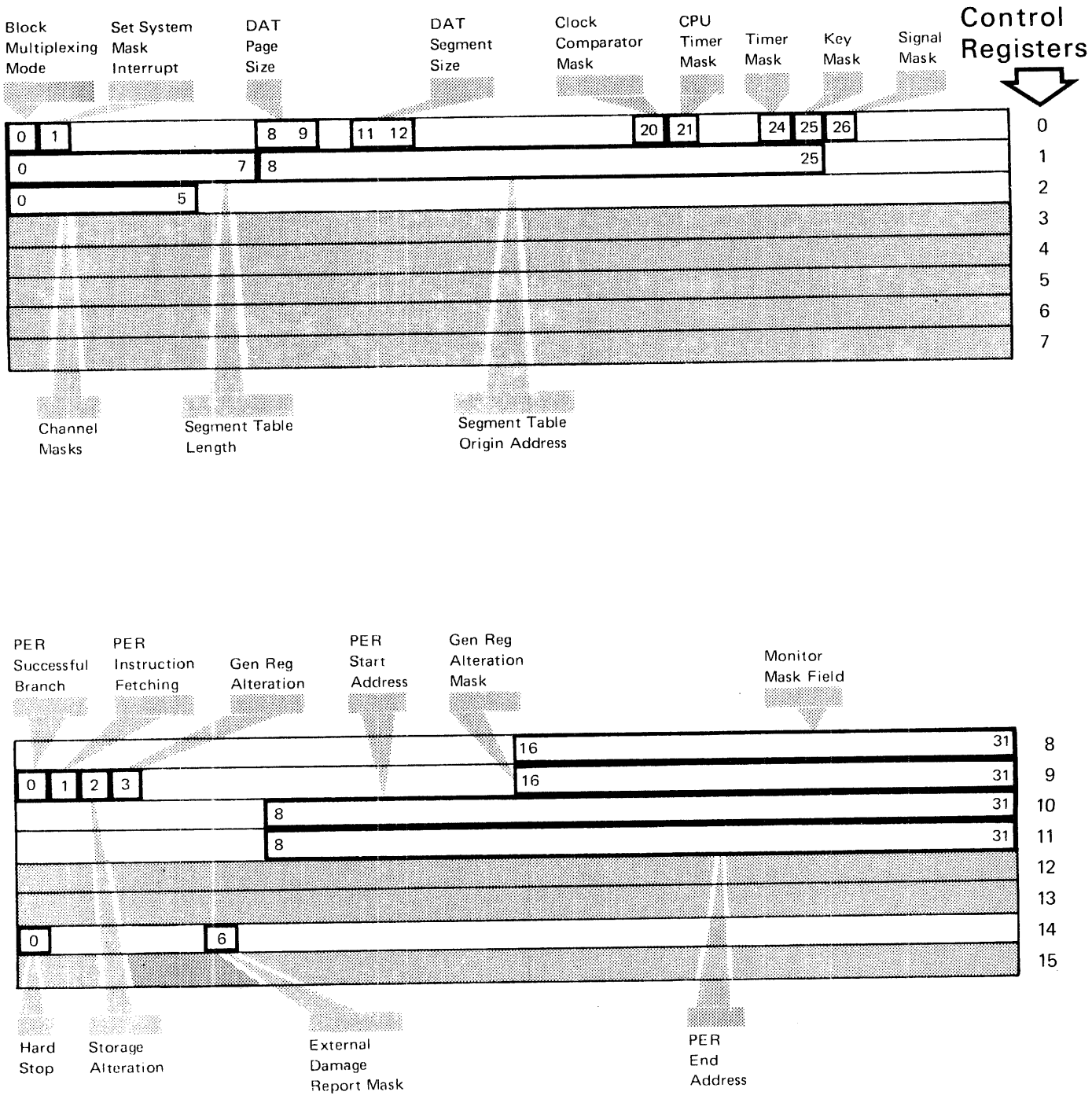
If the monitored register has been altered, or implicitly or explicitly designated as the destination, the address of the instruction responsible for the alteration or designation is recorded, and the updated instruction address is placed in the old PSW during the event interruption. Should the responsible instruction be the object of an 'Execute' instruction, the address of the 'execute' instruction is recorded.

Note: Program event recording applies to all System/360 and System/370 instructions, including 'do interpretive loop' (DIL). The emulator routines called via DIL are, however, not monitored explicitly. Because of this, a program event is indicated for any string of DIL instructions whenever the PER bit is on, whether or not the event occurred.

ERROR RECOVERY ENHANCEMENT

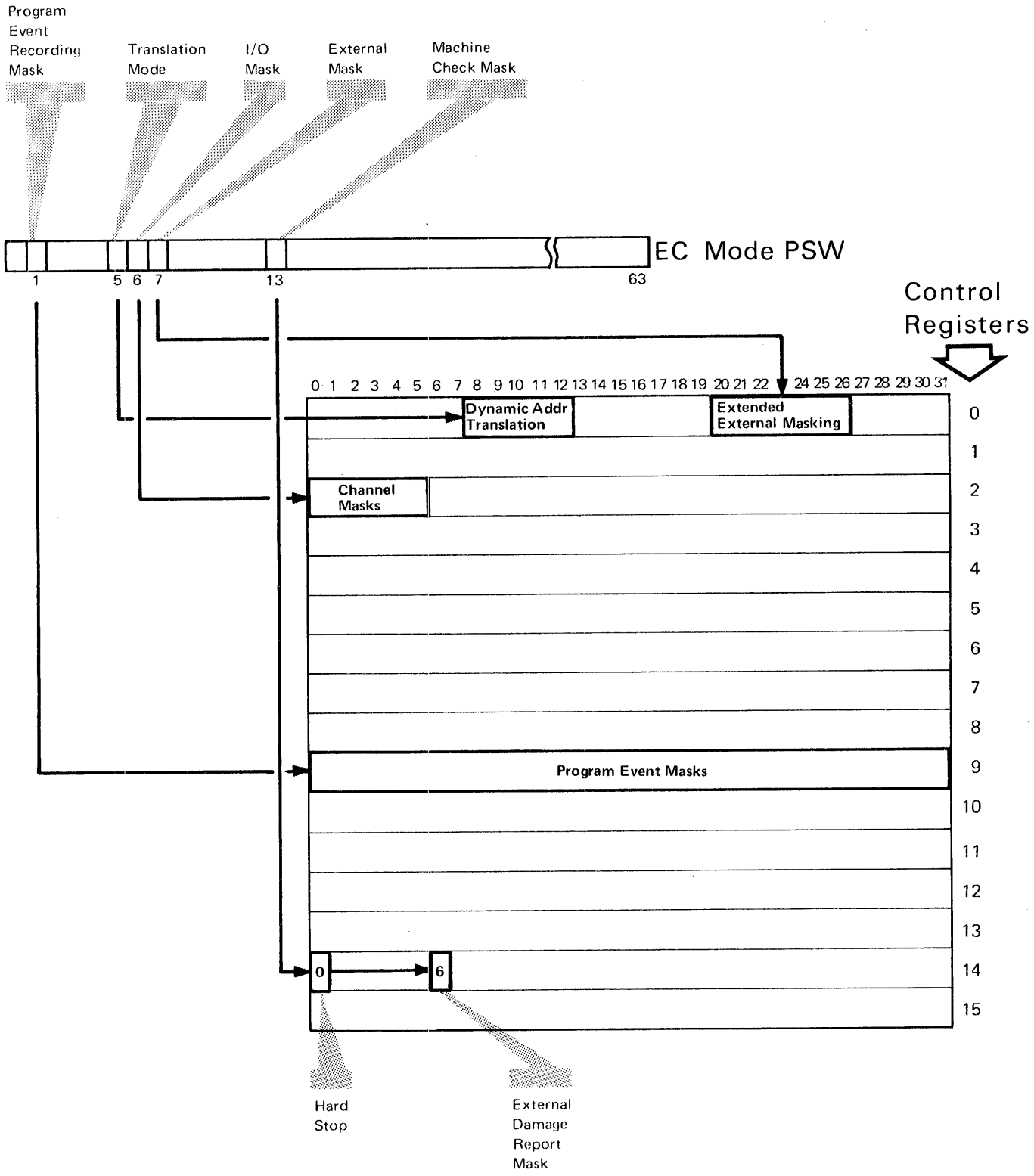
The Error Recovery Enhancement feature, which is a standard feature available in BC and EC mode, is handled through control register 14. Those error recovery functions implemented on the Model 115 are shown in Figure 23. The following functions, available on other System/370 models, are *not* implemented on the Model 115 because errors are logged and analyzed without the need for program support.

Bit	*Function (Not On Model 115)*
1	Synchronous machine-check Extended logout mask
2	Input/output extended logout mask
3	(Not assigned)
4	(Not used)
5	(Not used)
7	Warning mask
8	Asynchronous machine-check logout mask
9	Asynchronous fixed logout control



Control Registers Overview

Figure 16. Control Registers Overview [10795]



Relationship between EC Mode PSW Masks and Control Registers

Figure 17. Relationship between EC Mode PSW Masks and Control Registers [10796]

0 Block Multiplexing

1 = The direct disk attachment operates as a block multiplexer if the block multiplexing feature is installed.
0 = The block multiplexing feature (optional) on the direct disk attachment is disabled.

1 Set System Mask Interruption

1 = The 'set system mask' instruction is suppressed and an interruption occurs instead.
0 = The 'set system mask' instruction is executed normally.

8,9 DAT Page Size

If dynamic address translation is specified in the PSW, these bits specify the page size as follows:

Bit 8	*Bit 9*	
0	1	2,048 bytes
1	0	4,096 bytes (optional)

Other codes are invalid when DAT is on. The bits are ignored when DAT is off.

11,12 DAT Segment Size

If dynamic address translation is specified in the PSW, these bits specify the segment size as follows:

Bit 11	*Bit 12*	
0	0	65,536 bytes (64K)
1	0	1048,576 bytes (1 Mega) (optional)

Other codes are invalid when DAT is on. The bits are ignored when DAT is off.

20 Clock Comparator Mask

1 = An interruption will occur if the clock comparator value is less than the time-of-day (TOD) clock value, and PSW bit 7 is set.
0 = The interruption is disabled but remains pending as long as the comparator value is less than the TOD clock value. The interruption condition is removed if a greater value is set by the 'set clock comparator' instruction.

21 CPU Timer Mask

1 = An interruption can occur if the value in the CPU timer becomes negative, and PSW bit 7 is set.
0 = The interruption is disabled but remains pending as long as the value in the CPU timer is negative. If a positive value (zero is considered positive) is introduced, the interruption condition is removed.

24 Timer Mask

1 = An interruption can occur if the location 80 timer value becomes negative, and PSW bit 7 is set (in EC or BC mode).
0 = The interruption remains pending.

25 Key Mask

1 = An interruption can occur if the INTRPT (interrupt) key on the console keyboard is pressed, and PSW bit 7 is set (in EC or BC mode).
0 = The interruption remains pending.

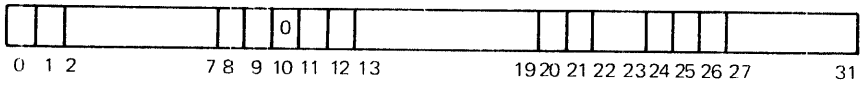
26 Signal Mask

1 = An interruption can occur from a condition in one or more of the six optional external signal lines, provided PSW bit 7 is set (in EC or BC mode).
0 = The interruption remains pending.

Effect of System Reset

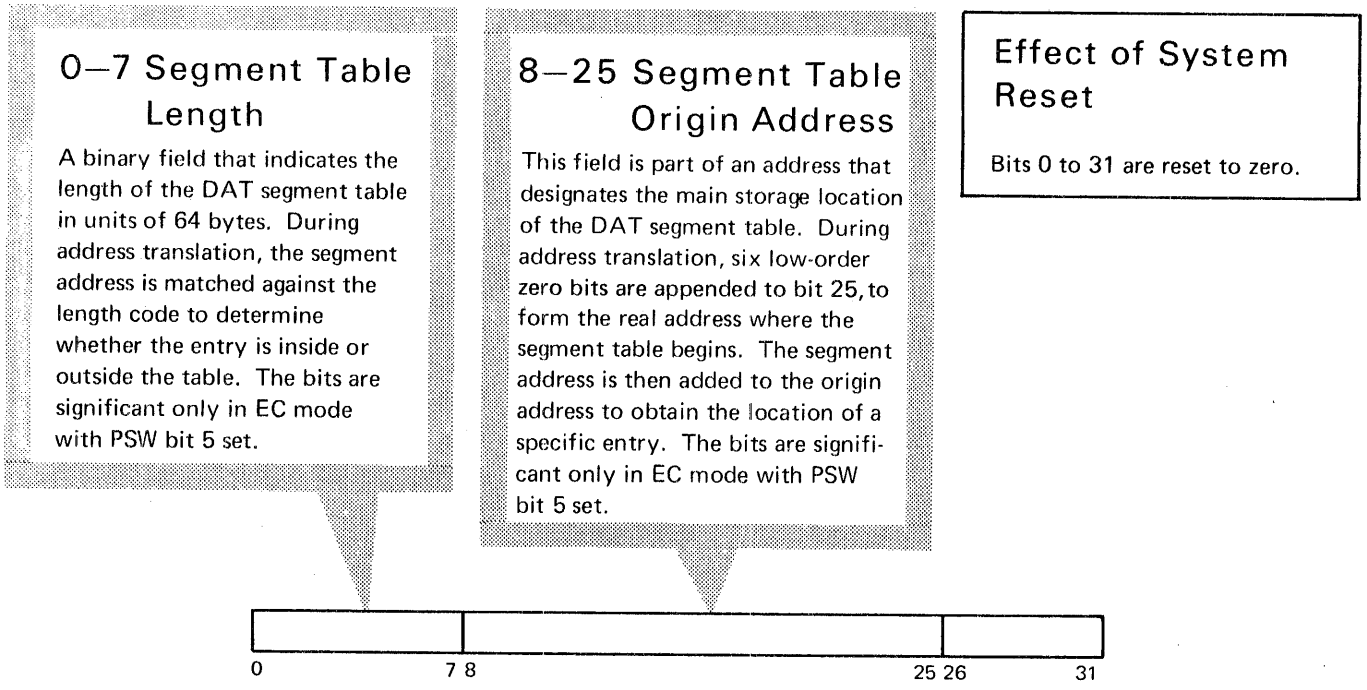
Bit	*Setting*	*Meaning*
0	0	Block multiplexing on disk is off.
8, 9	0	Page size is set to an invalid code.
10	0	Unassigned; must be zero.
11, 12	0	Segment size is set to 64K.
20	0	Clock comparator interruption is disabled.
21	0	CPU timer interruption is disabled.
24	1	Timer interruption is enabled.
25	1	INTRPT key is enabled.
26	1	External signal interruptions are enabled.

Unassigned bits are set to 0.



Control Register 0

Figure 18. Control Register 0 [10797]



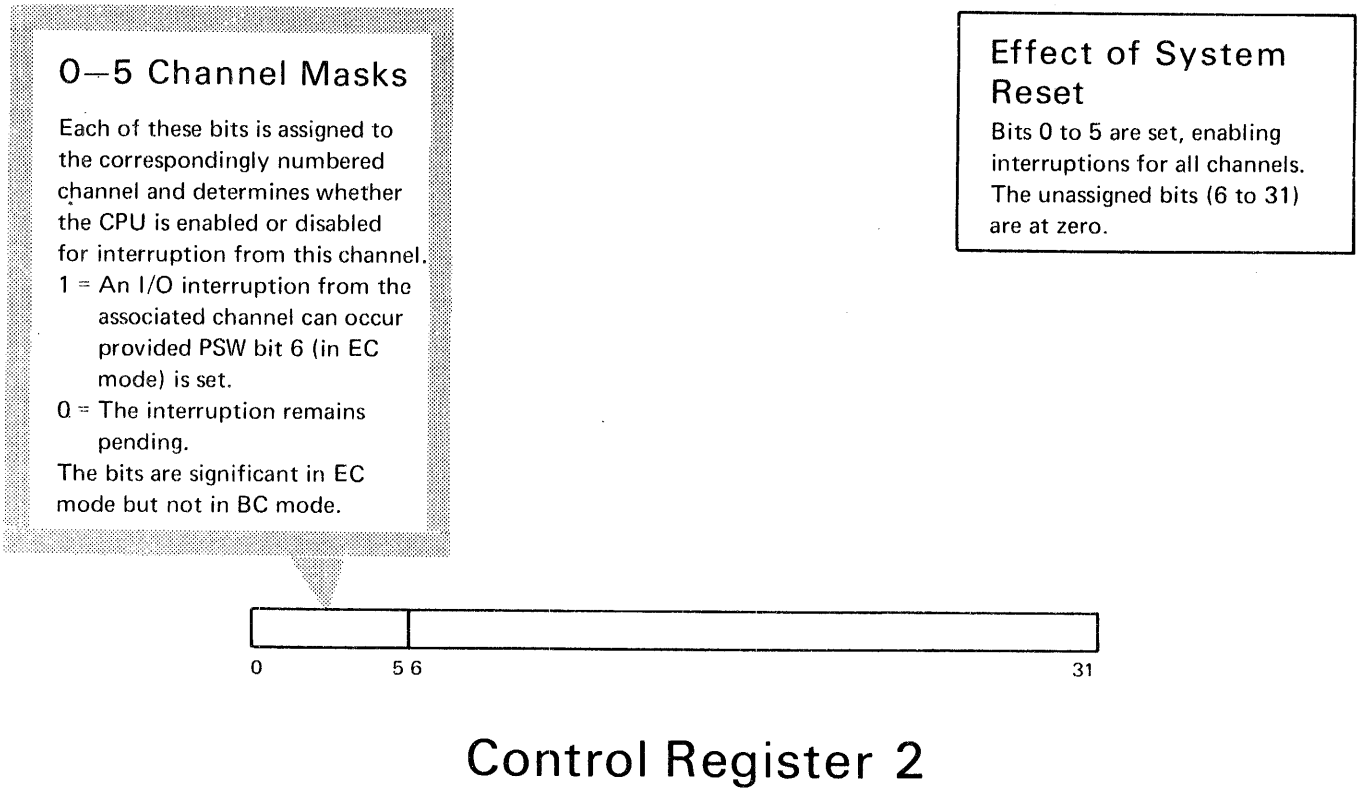
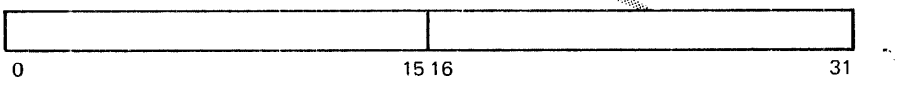


Figure 19. Control Registers 1 and 2 [10798]

16—31 Monitor Mask Field

Each bit represents a class of events, which is monitored when the bit is set. Bit addressing is done by a 'monitor call' instruction containing a monitor class number ranging from 0 to 15. Number 0 addresses mask bit 16, number 1 addresses mask bit 17, and so on. When a bit set at one is addressed, an interruption occurs; when a bit which is off is addressed there is no effect.



Effect of System Reset

All bits are reset to zero, thus switching monitoring off.

Control Register 8

Figure 20. Control Register 8 [10799]

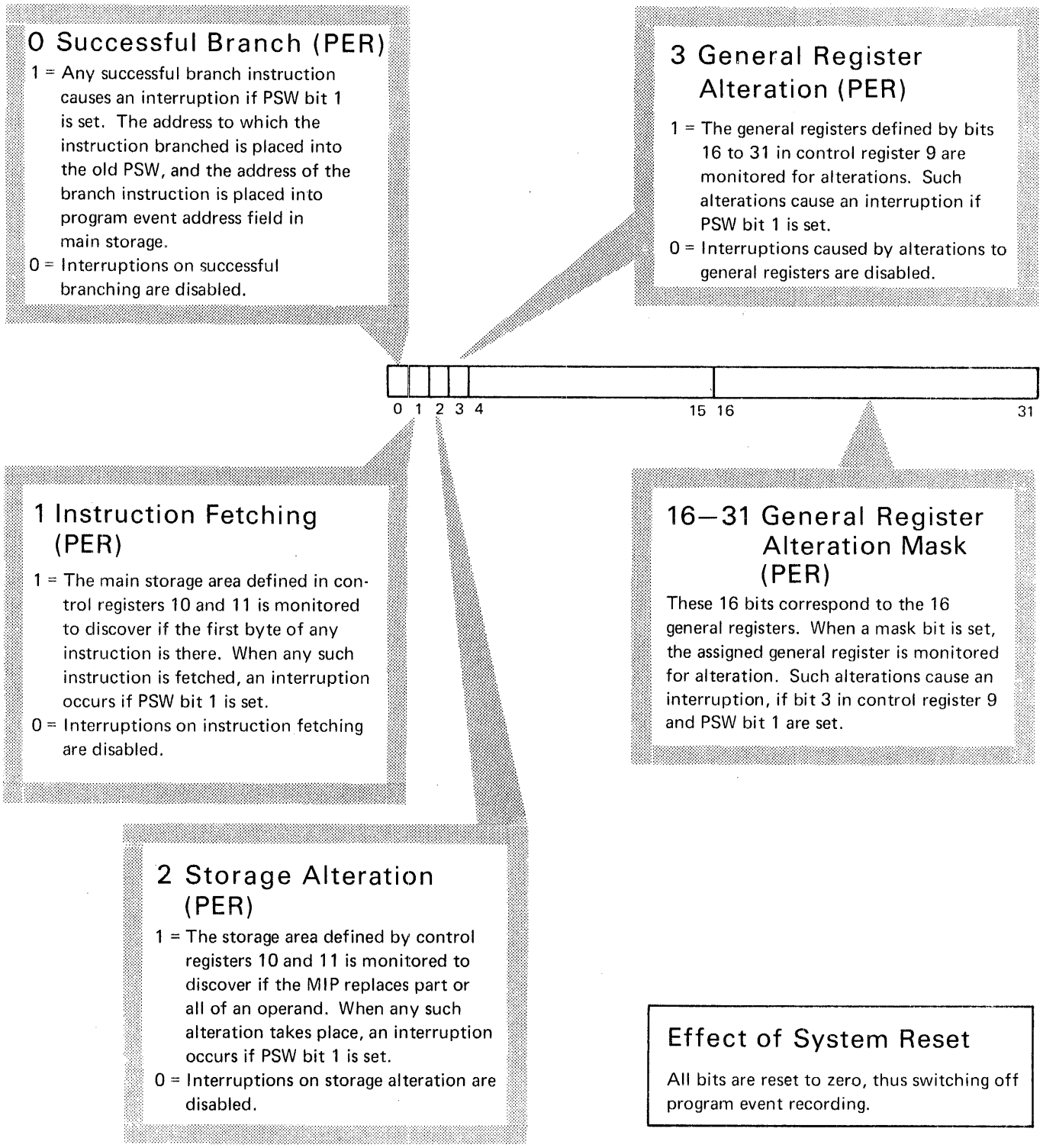


Figure 21. Control Register 9 [10800]

8—31 PER Start and End Addresses

These bits contain the start address (control register 10) and the end address (control register 11), which define the area in main storage to be monitored for two of the program events, instruction fetching and storage alteration. The addresses are both virtual. When both addresses are identical, only one location (byte) is monitored. If the start address is higher than the end address, monitoring extends to location 16,777,215, wraps around and continues from 0 through the end address.

Effect of System Reset

Both addresses are forced to zero.

Control Registers 10 and 11

Figure 22. Control Registers 10 and 11 [10801]

0 Hard Stop

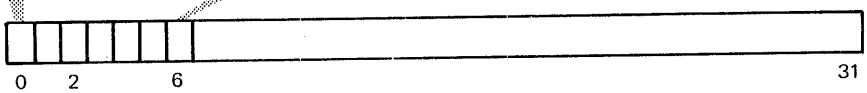
A 'hard' machine check condition causes the system to enter the check stop state, provided machine check interruptions are masked off (PSW bit 13 is 0). In the check stop state, the machine is stopped and the START key does not function. Recovery is by reloading the program.

Bit 0 is always treated as if it were turned on.

6 External Damage Report Mask

1 = An interruption reporting damage to the location 80 timer, the TOD clock, the CPU timer, the clock comparator, I/O attachments, channel, or other external sources can occur if PSW bit 13 is set.

0 = External damage interruptions cannot occur.



2 I/O Extended Logout Mask

Bit 2 has no function. The Model 115 performs no I/O extended logouts because errors are logged and analyzed without the need for program support. The bit may be set or at 0.

Effect of System Reset

Bit	*Set to*
0	1
2	0
6	1

Control Register 14

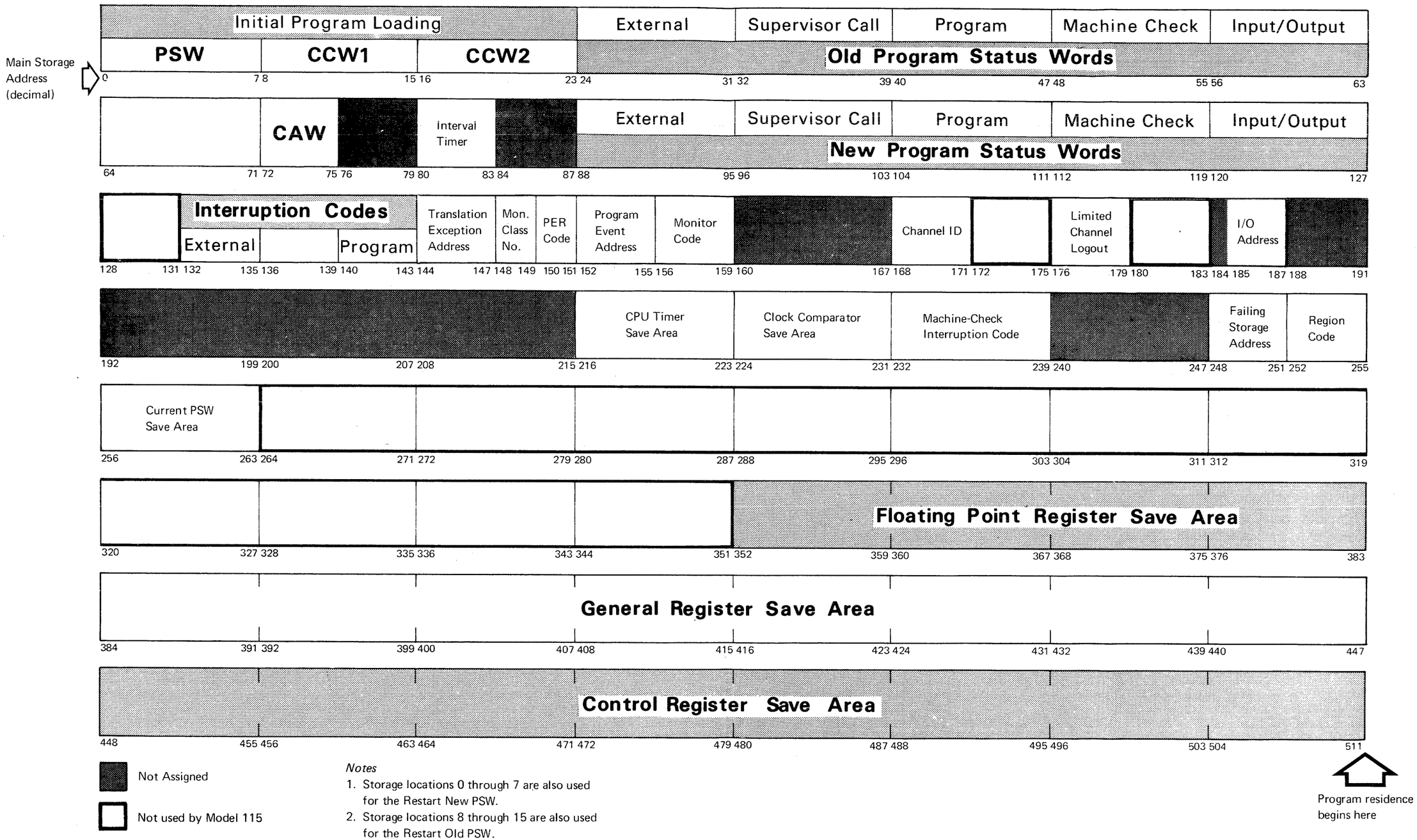
Figure 23. Control Register 14 [10802]

Fixed Areas in Main Storage

The fixed areas in main storage (Figures 24 to 31) are important for system control because they contain the various new and old program status words, and special reports which show, for example, channel error data. The areas are permanently allocated and the internal control mechanism of the Model 115 relies on this allocation.

MACHINE-CHECK LOGOUT

Instead of logging error information into fixed or extended main storage areas, the Model 115 logs detailed information about the nature of the malfunction onto its internal file. This log operation occurs whenever the interrogation loop (which runs continuously) detects an error condition. If such a condition is detected, a machine-check interruption is requested. For details of the machine-check interruption code see Figure 29; for details of limited channel logout see Figure 27.

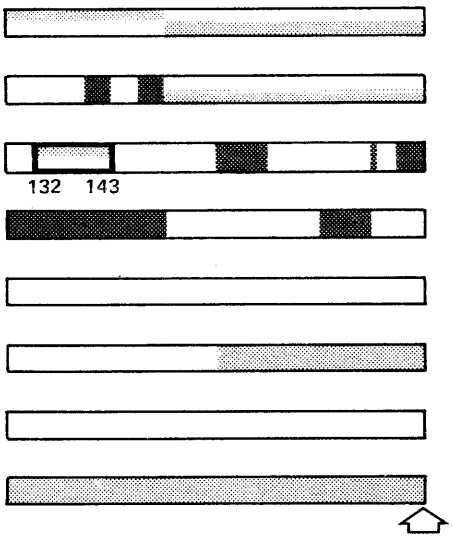


Notes

1. Storage locations 0 through 7 are also used for the Restart New PSW.
2. Storage locations 8 through 15 are also used for the Restart Old PSW.

Fixed Areas in Main Storage

Figure 24. Fixed Areas in Main Storage [10803]



Interruption Codes

External Interruption Code

132

0000000000000000 | Interruption Code

0 15 16 31

This storage location is used only when an external interruption occurs during operation in EC mode. If BC mode was specified, the code is placed into bits 16 to 31 of the external old PSW.

SVC Interruption Code

with Instruction Length Count

136

0000000000000 | 0 | Interruption Code

0 12 15 16 31

ILC

When EC mode is specified, the supervisor call (SVC) interruption code and the instruction length count are placed in storage location 136 to 139. In BC mode, the code is placed into bits 16 to 31 and 32 to 33 of the supervisor call old PSW.

Program Interruption Code

with Instruction Length Count

140

0000000000000 | 0 | Interruption Code

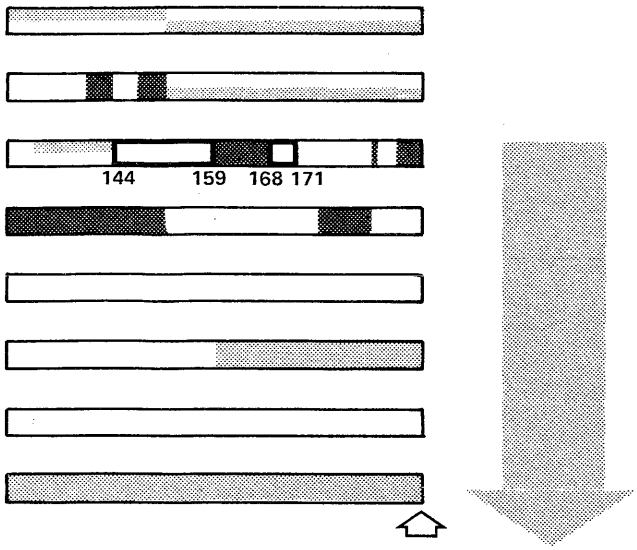
0 12 15 16 31

ILC

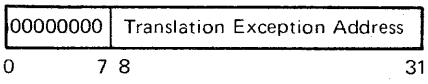
When EC mode is specified, the program interruption code and the instruction length count are placed in storage location 140 to 143. In BC mode, the code is placed into bits 16 to 31 and 32 to 33 of the program old PSW.

Main Storage Locations 132–143

Figure 25. Main Storage Locations 132–143 [10804]

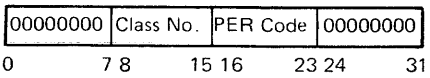


144—147 Translation Exception Address



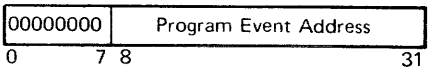
This field is used only when EC mode and dynamic address translation are on and the translation process ends with a segment translation or page translation exception interruption. The virtual address responsible is stored in location 144-147 and the interruption code identifies the exception.

148—151 Monitor Class Number and PER Code



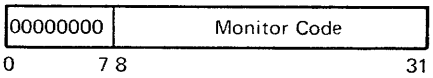
The monitor class number originates from the 'monitor call' instruction and corresponds to the monitor class bit found in the control register. The resulting interruption causes the class number to be stored.
The PER code corresponds to the program event control bit or bits in the control register. The bit is stored during an interruption to identify the event causing the interruption.

152—155 Program Event Address



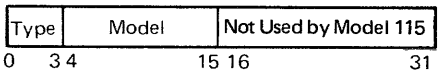
The program event address is stored during an interruption caused by a program event. The address points to the location of the instruction that caused the event (such as a general register alteration, a storage alteration, or a successful branch, etc.).

156—159 Monitor Code



During a monitor call interruption, the monitor code is stored to identify uniquely the monitored event. The code is the result of adding the contents of the base register (referenced in the 'monitor call' instruction) to the displacement provided by this instruction.

168—171 Channel Identification



This field is stored as the result of the 'store channel ID' instruction. The identification data is generated by adding the contents of the base register to the displacement provided by the 'store channel ID' instruction. The type field specifies:

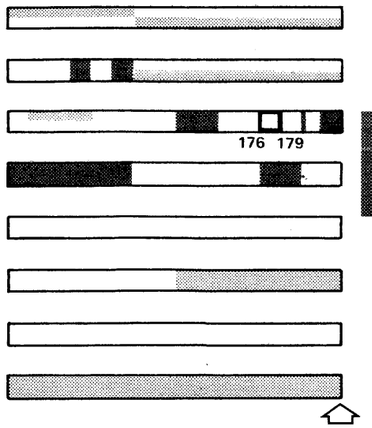
Selector Type	(0000)
Multiplexer	(0001)
Block Multiplexer	(0010)

The model number in bits 4-15 identifies the integrated adapters, attachments, and the channel as follows:

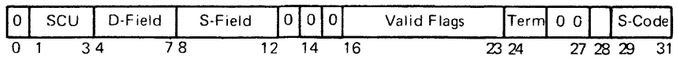
Hex Code	*Channel*
00C	0 (multiplexer)
00E	1 (direct disk attachment)
00D	2 (magnetic tape adapter)
00F	All integrated adapters and attachments in channel 0 (console, card I/O, line printer, ICA)

Main Storage Locations 144—171

Figure 26. Main Storage Locations 144—171 [10805]



176–179 Limited Channel Logout



The following uncorrectable channel errors cause this report to be generated:

- Channel Data Check
- Channel Control Check
- Interface Control Check

The limited channel logout is stored when the CSW is updated, provided the affected IOP is not damaged to an extent which prevents CSW-updating and logout storing. If the IOP is damaged, the SVP initiates an external damage interruption instead of a limited channel logout.

1–3 Storage Control Unit

These bits are at zero, indicating that the MSC was the unit through which the storage reference was directed when the error occurred. The Model 115 has no other storage control units.

4–7 Detect Field

The unit detecting the error is identified by the setting of one of the following bits:

Bit	*Designation*
4	CPU
5	Channel
6	Storage control unit
7	Storage

In the Model 115 the error is always detected by the channel.

8–12 Source Field

The most likely source of the error is indicated by the setting of one of the following bits:

Bit	*Designation*
8	CPU
9	Channel
10	Storage control unit
11	Storage unit
12	Control unit

In the Model 115 the most likely source will be either the channel or control unit.

16–23 Field Validity Flags

A field validity flag bit set at one indicates that the assigned field was stored with valid information. If a bit is zero, the assigned field is unpredictable. Assignments are:

Bit	*Designation*
16	Interface address (not applicable to Model 115
17, 18	Reserved
19	Sequence code
20	Unit status
21	Command address and key
22	Channel address
23	Device address

24–25 Type of Termination

These bits indicate how the affected channel operation was ended, as follows:

Bit Setting	*Meaning*
00	Interface disconnect
01	Stop, stack or normal termination
10	Selective reset
11	System reset

29–31 Sequence Code

The I/O sequence in progress when the error occurred is identified by the following bit settings:

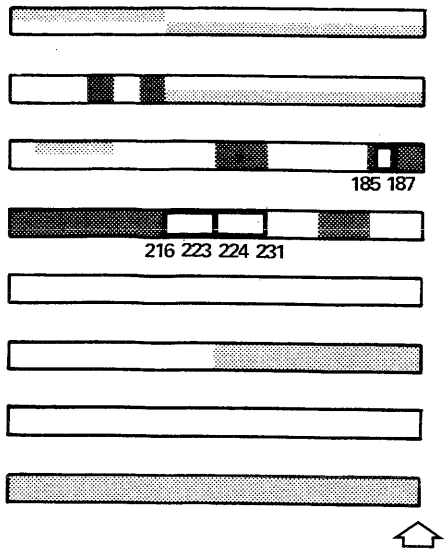
Bit Setting	*Meaning*
000	Execution of test I/O
001	Command byte went out but status not yet available
010	Command accepted but data transfer not yet started
011	At least one data byte already transferred
100	Command not yet sent or not accepted
101	Command accepted but data transfer unpredictable
110, 111	Reserved

Note: These codes are meaningless for 'halt I/O' or 'halt device' instructions.

Note: Bit 28 is not used by the Model 115

Main Storage Locations 176–179

Figure 27. Main Storage Locations 176–179 [10806]



185—187 I/O Address

During an I/O interruption in EC mode, the two-byte I/O address is stored at locations 186-187, and zeros are stored at location 185.

224—231 Clock Comparator Save Area

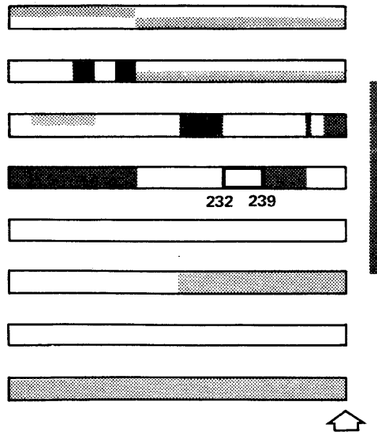
The contents of the clock comparator are stored in this area during a machine-check interruption, or when a store status operation is carried out by the operator.

216—223 CPU Timer Save Area

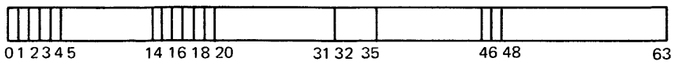
This location is used during a machine check interruption to save the contents of the CPU timer.

Main Storage Locations 184—231

Figure 28. Main Storage Locations 184—231 [10807]



232–239 Machine-Check Interruption Code



This code identifies the damage and gives information on the location and point in the program at which the condition caused the interruption. A machine-check interruption is requested only after internal logging has been completed. The code is stored in locations 232 to 239 when the machine-check interruption occurs.

Note: If the machine-check interruption code cannot be stored or the interruption cannot be executed, the system enters the check stop state.

0 System Damage

This bit is set to indicate uncorrectable errors in one of the following units or functions:

- MIP
- MSC control circuitry
- Interruption system (leading to loss of interruptions)
- Direct disk attachment (parity errors affecting MIP).

These are hard errors causing entry into the check stop state.

1 Instruction Processing Damage

This bit is set to indicate uncorrectable parity errors as follows:

- In MIP
- From main storage to MIP
- In addresses.

Processing damage is a hard condition causing entry into the check stop state.

2 System Recovery

This bit is set to indicate that automatic recovery (made after detection of an error) was successful.

3 Timer Damage

This bit is set to indicate an uncorrectable error in the location 80 timer.

4 Timing Facilities Damage

This bit is set to indicate damage to the TOD clock, clock comparator or CPU timer.

5 External Damage

This bit is set to indicate an uncorrectable error in an IOP or its attachment, or in the SVP. A limited channel logout may be available.

14 Backup

1 = The instruction address in the machine-check old PSW refers to the instruction that caused the error, or was being executed when the error was detected.

0 = The address in the machine-check old PSW points to an instruction located beyond the point of error detection.

15 Delayed

This bit is set when the machine-check interruption was delayed, because machine checks were masked off at the time of request.

16 Storage Error

This bit, when set, indicates that a storage reference caused the detection of uncorrectable damaged data. (For example, a double-bit error in a storage with automatic correction for single-bit errors.)

17 Storage Error Corrected

This bit, when set, indicates that a storage reference resulted in an error that was corrected.

18 Storage Key Error Uncorrected

This bit, when set, indicates that a storage reference caused the detection of an uncorrectable key error. Storage keys are checked for errors only when the PSW or CAW key is non-zero.

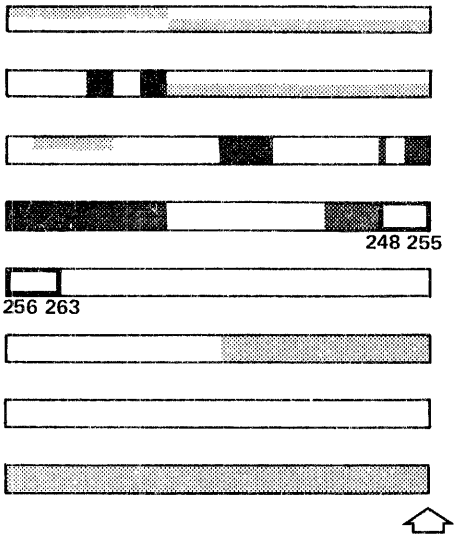
20–63 Machine-Check Interruption Code Validity Bits

These bits indicate the reliability of information stored during a machine-check interruption. The degree of damage so far caused can be assessed by evaluating these bits whose meanings, when set, are as follows:

Bit	*Meaning*
20	Bits 12 to 15 of machine-check old PSW are valid
21	PSW masks and key of machine-check old PSW valid
22	Program mask and condition code valid in old PSW
23	Instruction address valid in old PSW
24	Failing storage address valid (in storage)
25	Region code valid (in storage)
26	Always 0
27	Floating point registers valid (in storage)
28	General purpose registers valid (in storage)
29	Control registers valid (in storage)
30	(Not used)
31	Storage area prior to interruption point valid
32–45	(Not used)
46	CPU timer saved valid
47	Clock comparator
48–63	(Not used).

Main Storage Locations 232–239

Figure 29. Main Storage Locations 232–239 [10808]



248–251 Failing Storage Address

00000000	Failing Storage Address

0 7 8 31

During a machine-check interruption, this area is used to record the address of the failing storage location if an uncorrectable storage error occurs.

252–255 Region Code

Channel	Device	Not Used

0 7 8 15 16 31

The region code is stored during a machine-check interruption that is caused by external damage. The code identifies the affected IOP, and therefore also identifies the native attachment or channel (or the timing facility).

Bits 0 to 15 provide the following information:

Hex code	*Meaning*
N00E	Card I/O and printer
N01F	Video console
N020	Telecommunications
N0F0	Multiplexer channel
N100	Disk attachment
N200	Tape adapter
003A	Timer facilities
003B	External signals

N = 0 if damage occurred during I/O instruction.

N = 1 if damage occurred during interrupt handling.

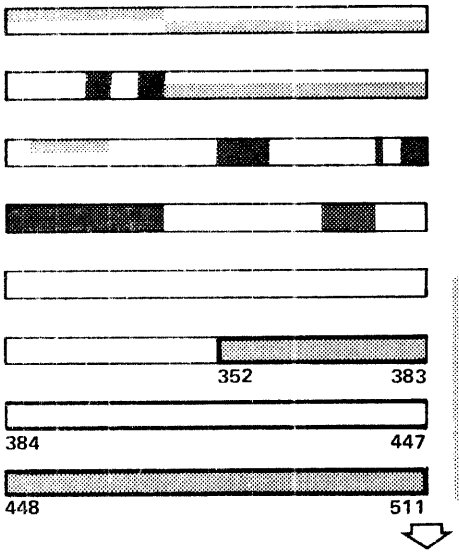
The device address from the instruction is used in the region code if it is available, otherwise the addresses listed above are used.

256–263 Current PSW Save Area

The current PSW is stored in this area when the operator carries out a store status operation.

Main Storage Locations 248–263

Figure 30. Main Storage Locations 248–263 [10809]



352—383 Floating Point Register Save Area

If a machine-check interruption occurs, the CPU attempts to save the contents of all floating point registers (if floating point feature is installed) into this area. If none or only part of the registers can be saved, the validity bit in the machine-check interruption code will be zero.

384—447 General Register Save Area

During a machine-check interruption, the CPU attempts to save the contents of all general registers.

Note on Register Saving

If the MIP is damaged, the task of saving registers is delegated to the SVP. If the SVP is unsuccessful, system damage is indicated. The validity bits in the machine-check interruption code show the extent to which saving was successful.

448—511 Control Register Save Area

During a machine-check interruption, the CPU attempts to save the contents of all control registers.

Main Storage Locations 352—511

Figure 31. Main Storage Locations 352–511 [10810]

Interruption Mechanism

The interruption mechanism of the Model 115 is logically the same as that of the System/360 except for handling differences in EC mode and the extra information available in certain new types of program interruptions. An interruption consists of storing the current PSW into a main storage location where it becomes the old PSW, and fetching a new PSW which is set up as the current PSW. Processing then continues in the state and at the instruction address introduced by this PSW. The old PSW contains the address of the instruction which would have been executed next if the interruption had not occurred, and also the interruption code (bits 16 to 31) if BC mode is set. In EC mode, the interruption codes have fixed main storage allocations as shown in Figure 24.

The following types of interruptions, defined in *IBM System/370 Principles of Operation*, GA22-7000, are recognized by the Model 115:

- Input/Output interruptions
- Program interruptions
- Supervisor call interruptions
- External interruptions
- Machine check interruptions.

The following new types of program interruptions in the Model 115 (Figure 32) provide additional information:

- Monitor interruptions
- Program event recording interruptions
- Translation exception interruptions
- CPU timer interruptions
- Clock comparator interruptions.

Type of Interruption	Code Stored (Hexadecimal)	Main Storage Location (Decimal) where code is stored	Operating Mode in which the interruption occurs
DAT segment translation exception	Interruption code 0010	142–143	EC only
DAT page translation exception	Interruption code 0011		
DAT specification exception	Interruption code 0012		
Monitor	Monitor code	156–159	EC and BC
	Monitor class number	148–149	
Program event recording	Program event code	150–151	EC only
	Program event address	152–155	
Input/output	I/O address	185–187	EC only
	Limited channel logout	176–179	EC and BC, when channel data check, channel control check, or interface control check is set
Machine check	Interruption code	232–239	EC and BC
	Failing storage address (depending on error)	248–251	
	Contents of floating point, general, and control registers	352–511	
CPU timer	Interruption code	132–135	EC
		Old PSW bits 16–31	BC
Clock comparator	Interruption code	132–135	EC
		Old PSW bits 16–31	BC

Figure 32. Additional Information on Interruptions [10811]

Timers

A time-of-day clock, two timers, and a clock comparator (Figures 33 to 36) are available as standard features on the 3115. The TOD clock measures elapsed time; the timers and the clock comparator provide program-controlled interruptions.

These interruptions, which are classed as external interruptions, are enabled, disabled, or left pending according to the setting of the external mask (PSW bit 7) and the appropriate bits in control register 0 (see Figure 18). If the external mask bit and the relevant timer mask bit are set, timer interruptions are enabled. If the external mask bit or the relevant timer mask bit is zero, timer interruptions are disabled, except for location 80 timer interruptions which remain pending.

As most of the timing facilities are not located in main storage, special instructions are provided for the programmer to examine or change the contents of timer locations. An exception is the interval timer at main storage location 80, which can be addressed by any suitable instruction that has location 80 as an operand.

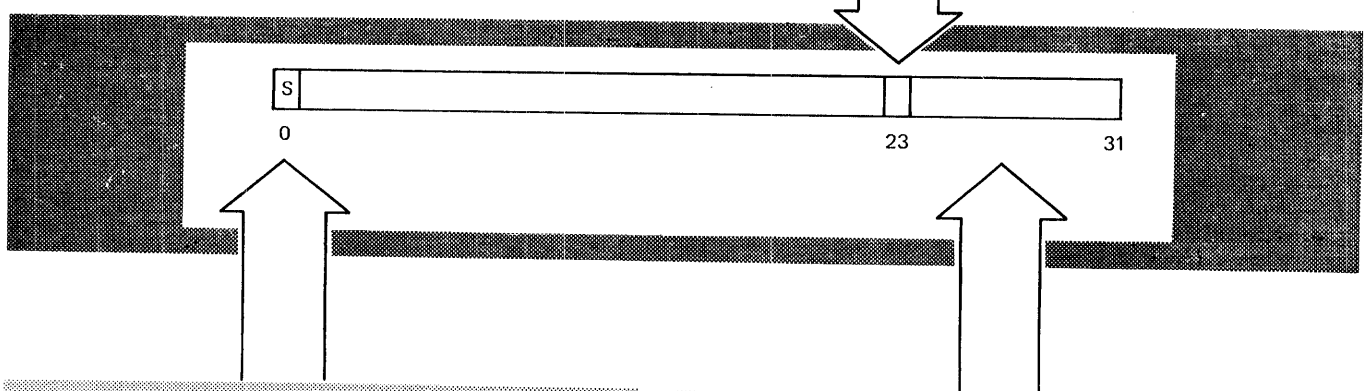
The timer is a 32-bit word at main storage location 80. Suitable instructions, designating location 80 as an operand, can store a value into or fetch a value from the timer at any time, provided location 80 is not protected against those operations.

The data in the timer is interpreted as a signed binary integer. Fetching from or storing into location 80 is interlocked to prevent collision with updating or with carry propagation. The updating of the timer causes internal performance degradation of 0.4%.

Updating

When the system is in run mode, bit position 23 is decremented by one every 3.33 milliseconds (ms). If higher priority requests prevent the MIP from accessing main storage, the next update compensates for the delay. Updating stops when the system is stopped or in the check-stop state. Updating is also suspended during manual operations that cause the Model 115 to stop, such as alter/display. In the wait state, however, the timer runs.

System reset normal does not change the timer data, but system reset clear resets the location 80 timer with valid parity.



Sign Change

An interruption is requested in EC or BC mode when the count goes from positive to negative if the external mask (PSW bit 7) and the timer subclass mask (bit 24 in control register 0) are both set. If the timer is masked off, the interruption remains pending (even if a positive value is introduced).

Ignored

Bit positions 24 to 31 do not participate in updating, and data placed in these positions remains unchanged.

Location 80 Timer

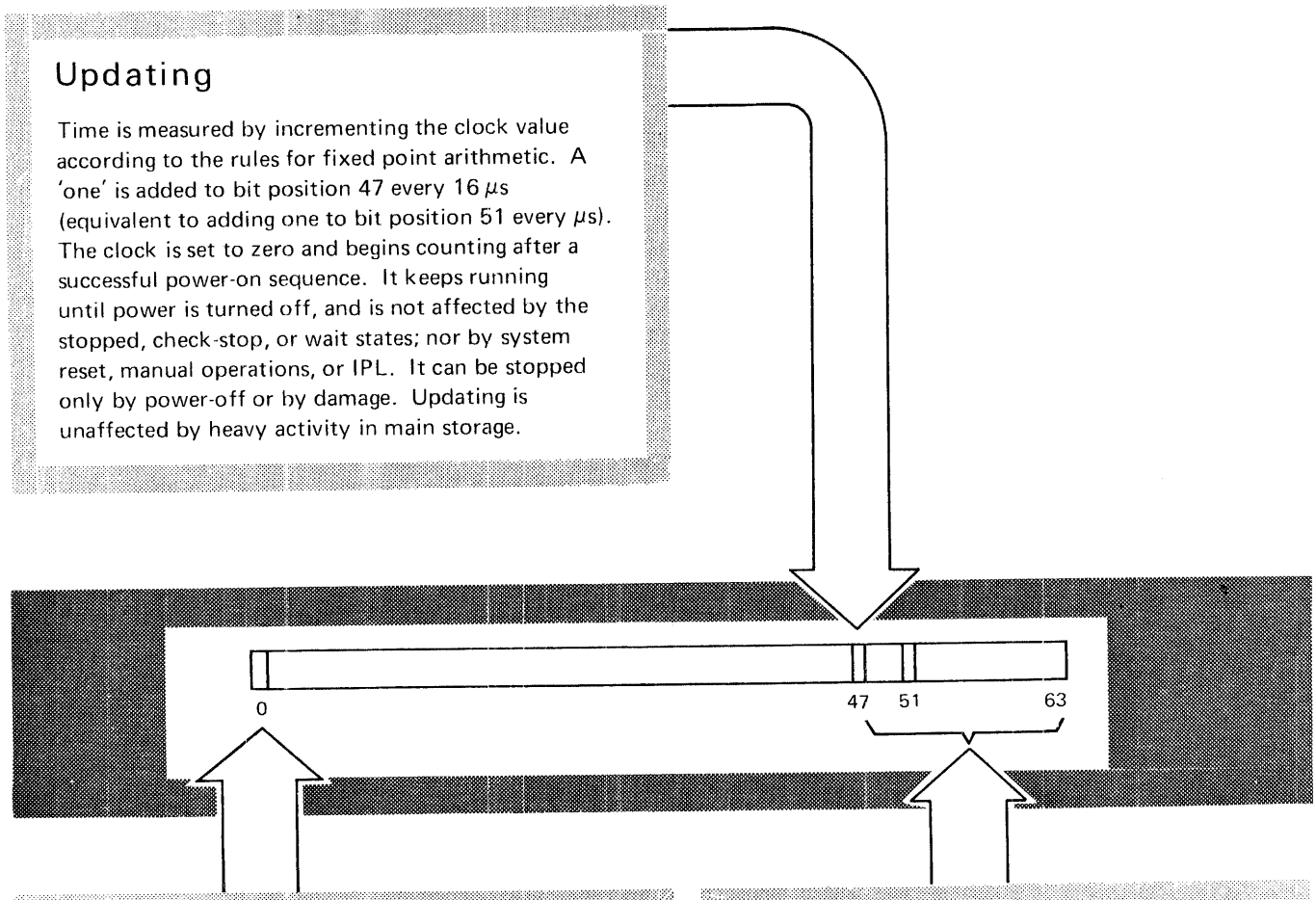
Figure 33. Location 80 Timer [10812]

The time-of-day clock is a doubleword binary counter, with contents corresponding to a fixed point number of double precision. The clock is not located in main storage. Its contents can be inspected by the 'store clock' instruction. The clock has a resolution of 16 μs, but successive instructions of this kind each store a unique clock value.

The clock value can be changed by the 'set clock' instruction. This instruction only works successfully, however, if the clock security switch at the operator console is simultaneously held to the ENBL SET position. This safeguards against accidental resetting. The success or failure of the 'set clock' instruction is indicated in the PSW condition code.

Updating

Time is measured by incrementing the clock value according to the rules for fixed point arithmetic. A 'one' is added to bit position 47 every 16 μs (equivalent to adding one to bit position 51 every μs). The clock is set to zero and begins counting after a successful power-on sequence. It keeps running until power is turned off, and is not affected by the stopped, check-stop, or wait states; nor by system reset, manual operations, or IPL. It can be stopped only by power-off or by damage. Updating is unaffected by heavy activity in main storage.



Effect of Carry

No interruption takes place when the clock is full, that is, a carry emerges from bit position 0. This carry is ignored, and counting continues from 0 onwards.

Ignored

Bit positions 48 to 63 do not participate in updating because they are physically non-existent. Therefore, a 'store clock' instruction cannot retrieve data from these positions, and a 'set clock' instruction cannot place data there.

Time-of-Day Clock

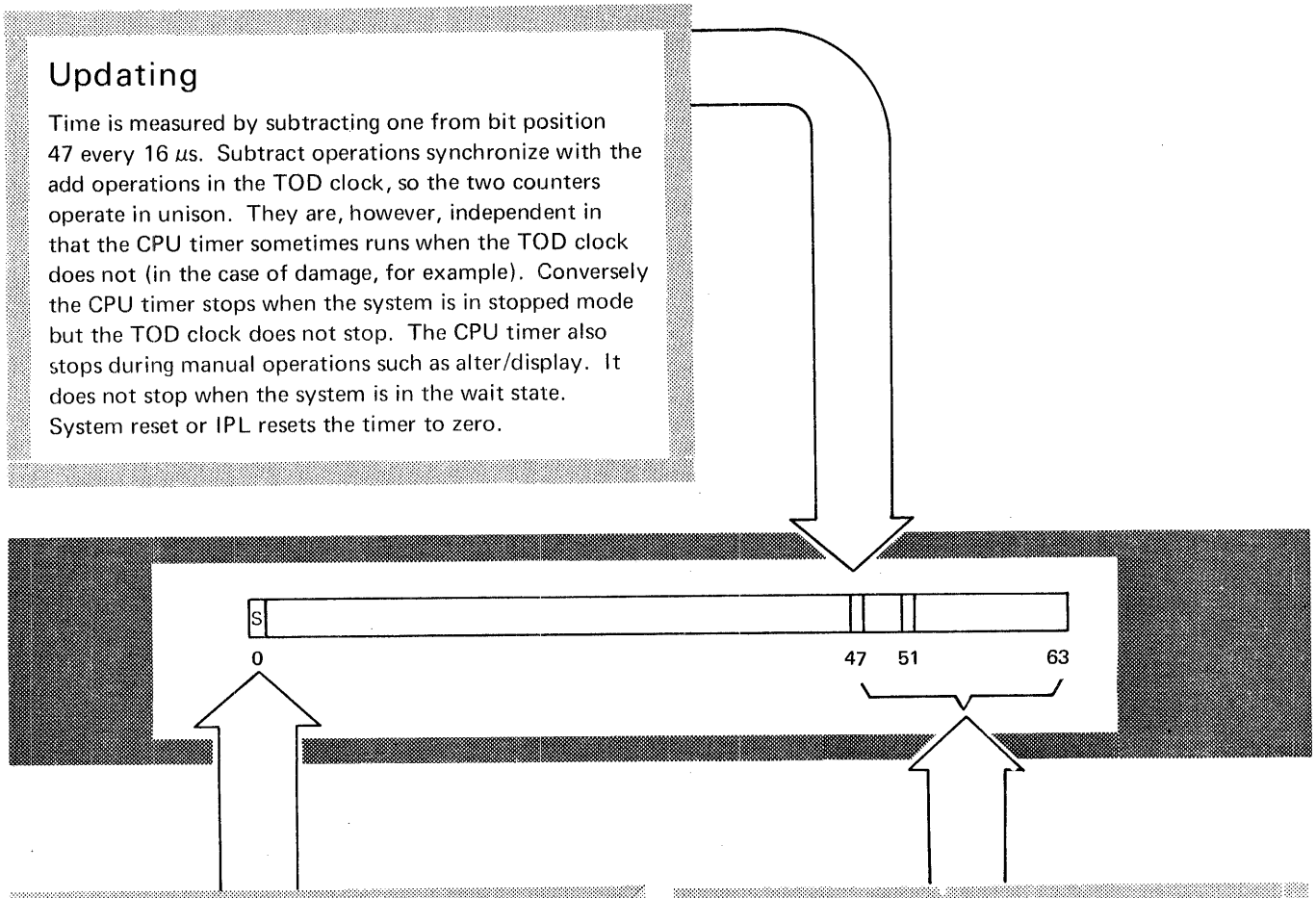
Figure 34. Time-of-Day Clock [10813]

The CPU timer is a binary counter with the same format as the time-of-day clock. It is not located in main storage. Its contents can be retrieved by the 'store CPU timer' instruction. Successive instructions of this kind each store a unique value into main storage.

The CPU timer value can be changed by the 'set CPU timer' instruction at any time without removing an interlock (there is no associated switch).

Updating

Time is measured by subtracting one from bit position 47 every 16 μs. Subtract operations synchronize with the add operations in the TOD clock, so the two counters operate in unison. They are, however, independent in that the CPU timer sometimes runs when the TOD clock does not (in the case of damage, for example). Conversely the CPU timer stops when the system is in stopped mode but the TOD clock does not stop. The CPU timer also stops during manual operations such as alter/display. It does not stop when the system is in the wait state. System reset or IPL resets the timer to zero.



Sign Change

An interruption condition is created in EC or BC mode when the count is negative. The interruption occurs if the external mask (PSW bit 7) and the CPU timer subclass mask (bit 21 in control register 0) are set while the timer is negative. If a positive value is set before the interruption is taken, the interruption condition is removed.

Ignored

Bit positions 48–63 do not physically exist and no data can be stored into or fetched from these positions.

CPU Timer

Figure 35. CPU Timer [10814]

Purpose

The clock comparator is used to cause an interruption when the value of the TOD clock reaches or passes a value specified in the program.

Setting

The clock comparator is set by the 'set clock comparator' instruction.

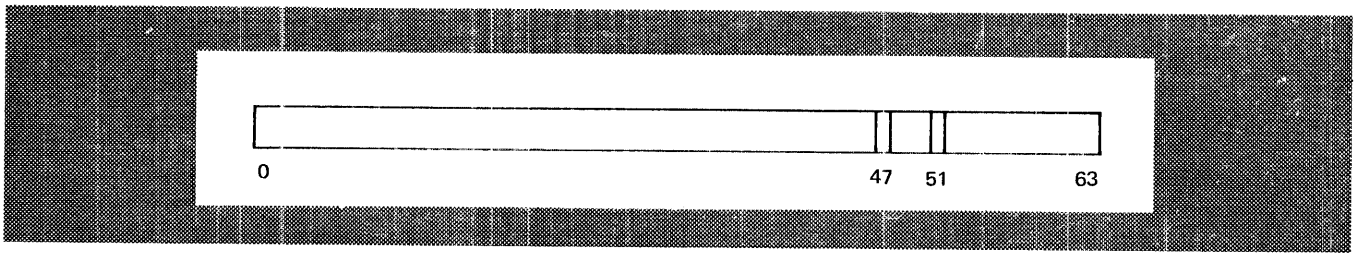
Inspection of Contents

The contents of the clock comparator can be inspected by means of the 'store clock comparator' instruction.

Interruptions

The 48 bits of the clock comparator represent an unsigned binary integer matching the size of the TOD clock. The comparator value is compared continuously with the TOD clock values, even if the system is in the stopped, check-stop, or wait state.

An interruption condition occurs whenever the comparator value is smaller than the TOD clock value, regardless of whether the clock is running, or in the error state. The interruption takes place if the external mask (PSW bit 7) and the comparator subclass mask (bit 20 in control register 0) are set. The condition is removed if a larger value is introduced by a 'set clock comparator' instruction before the interruption has occurred.



Resetting

System reset or IPL resets the clock comparator to zero.

Clock Comparator

Figure 36. Clock Comparator [10815]

Operator Console

The operator console (Figures 37 to 48), consisting of a video display and keyboard with control panel, is the means by which the operator can control the Model 115. The operator console replaces the conventional machine panel equipped with switches and lights.

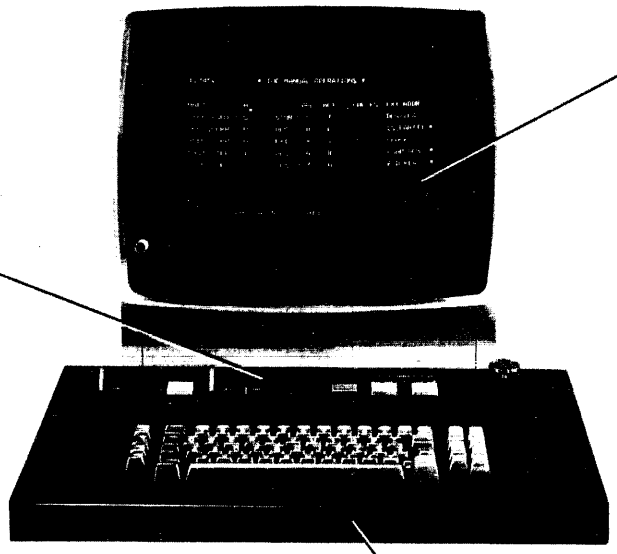
Manual operations (such as displaying and altering data, loading programs, and running the system in instruction step or address compare mode) are performed by keying selector characters from the keyboard into displays on the video screen. The screen is used to display all actions. There are no indicator lights to be decoded, because all information is displayed on the screen, in clear text, hexadecimal notation, or binary zeros and ones. A console printer is available, as an optional feature, to record messages as hard copy.

When the console is not being used as an operator panel, it is available to the operating system for displaying messages, and receiving responses from the operator.

A permanent display of the 3115 status is provided on the lower part of the video screen.

The Model 115's operator console is a standard integrated feature which allows:

- Communication between the operator and the system
- Manual control of events within the system.



Video Screen

The video screen displays keyboard input and messages from the operating system

Control Panel

The control panel contains keys and lights for functions which cannot be handled conveniently by the video display and keyboard

Console Keyboard

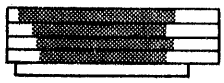
The console keyboard is used for keying information into the system, starting and stopping programs, and so on

Operator Console

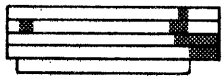
Figure 37. Operator Console [10816]

The console keyboard allows the operator to communicate with the system. Most of its functions are available in the stopped and in the running states of the system. There are three types of keys:

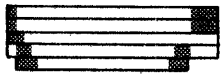
Alphameric Keys

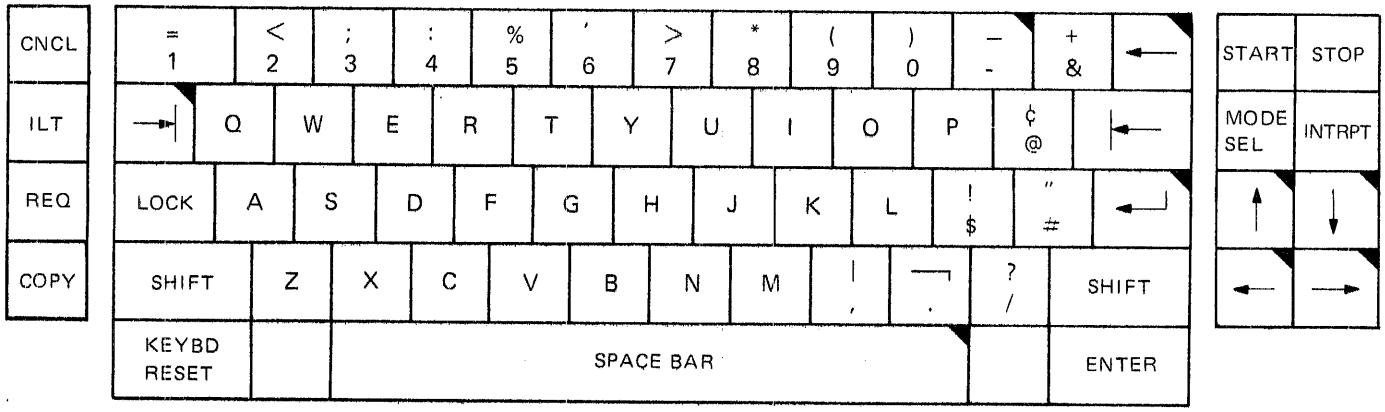


Cursor, Backspace, and Tabulator Keys



Function Keys





Legend

Typamatic action

Note: The space bar is not marked on actual keyboard.

Keyboard Disable Action

Locking is electrical, not mechanical, so locked keys can still be physically operated but no action results.

Keys which lock:

- All alphameric keys (including shift, space, backspace).
- ENTER
- COPY

Keys which do not lock:

- START
- INTRPT
- MODE SEL
- ILT
- CNCL
- REQ
- Cursor keys

Console Keyboard

Figure 38. Console Keyboard [10817]

The 45 alphameric keys, in conjunction with the shift keys, allow a total of 63 EBCDIC codes to be generated.

Nearly all the alphameric keys have momentary action: however long the key is pressed, only one character enters. The space bar and minus key are exceptions, being typamatic keys which cause one character to be entered when briefly pressed, and repetitive entry when held down.

A typed-in character does not enter the system until the ENTER key is pressed. Key selection errors can be corrected by overwriting before the entry is finalized.

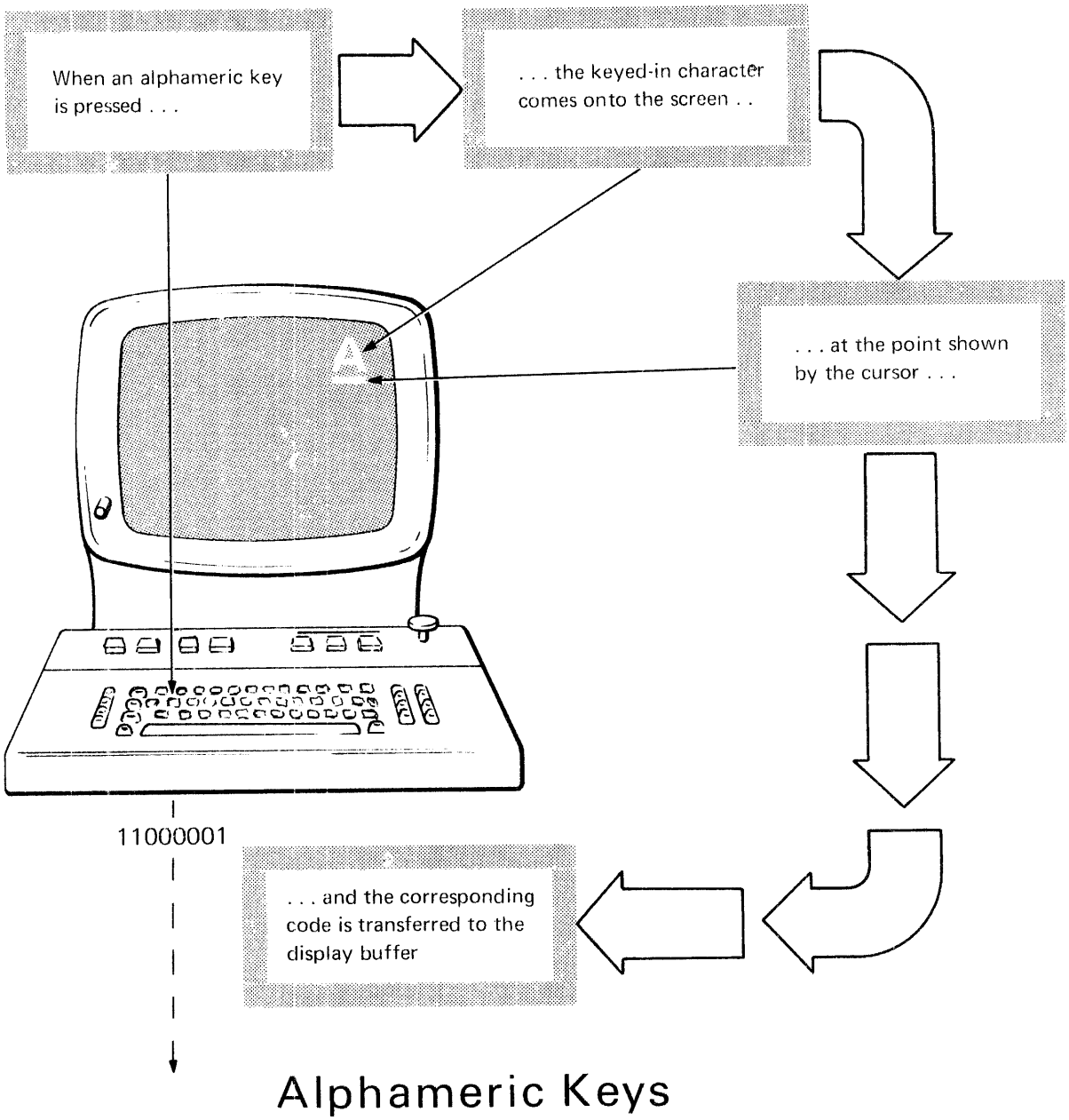
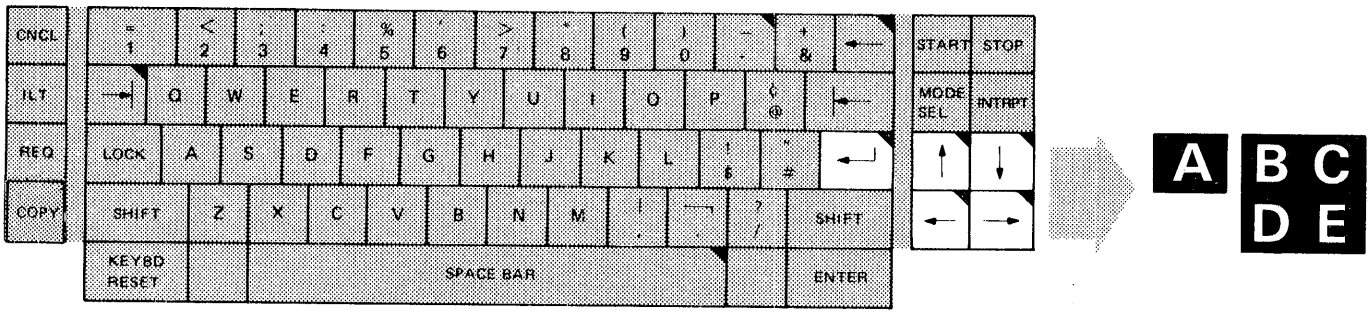
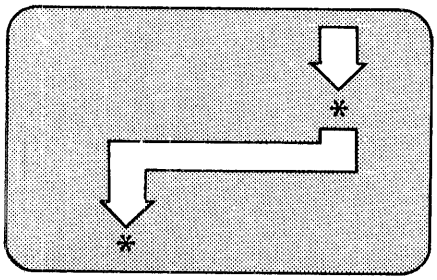


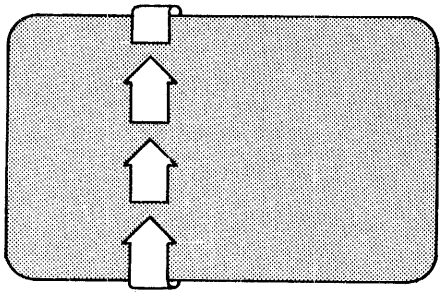
Figure 39. Alphameric Keys [10818]





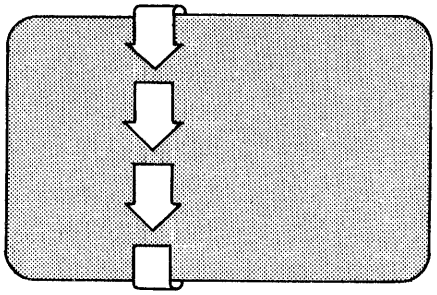
A Cursor to New Line

When the key is held down, the cursor moves to the first unprotected character position (*) in the first line down to have such an unprotected position, and so on, until a scan of all such lines has been made. On reaching the bottom of the screen, the cursor wraps to the first line with an unprotected character position.



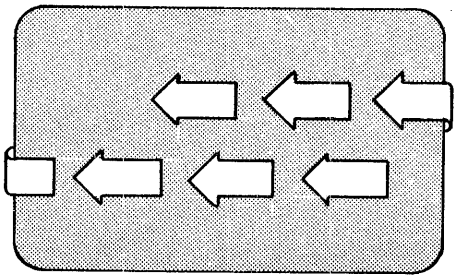
B Cursor Up

The cursor runs upwards, but stays in the same character column. On reaching the top of the screen, it wraps to the bottom and continues upwards again.



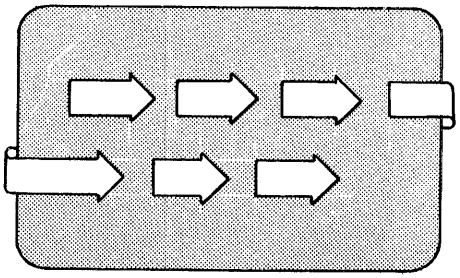
C Cursor Down

The cursor runs downwards but stays in the same character column. On reaching the bottom of the screen, it wraps to the top and continues downwards again.



D Cursor to Left

The cursor scans right-to-left, progressing up the screen. On reaching the top left-hand corner of the screen, it wraps to the bottom right-hand position and continues scanning.

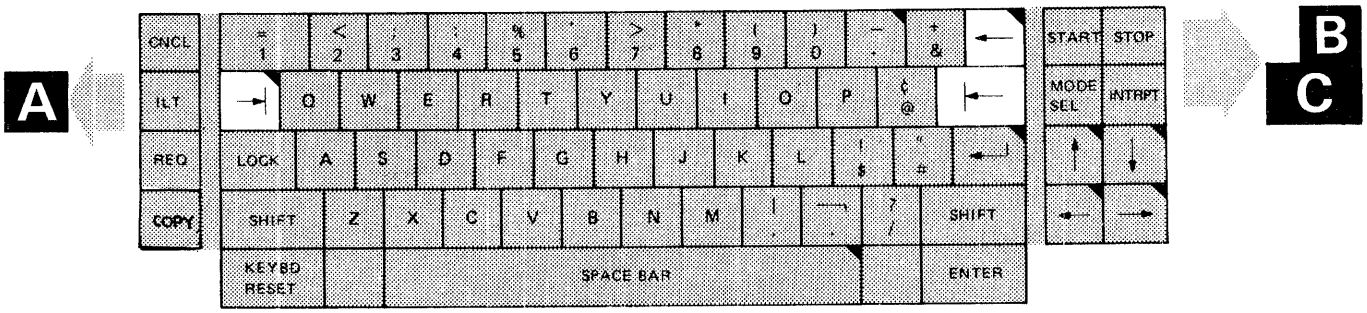


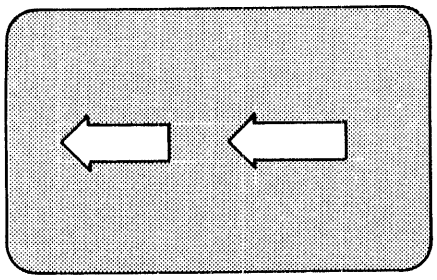
E Cursor to Right

The cursor scans left-to-right, progressing down the screen. On reaching the bottom right-hand corner of the screen, it wraps to the top left-hand position and continues scanning.

Cursor Control

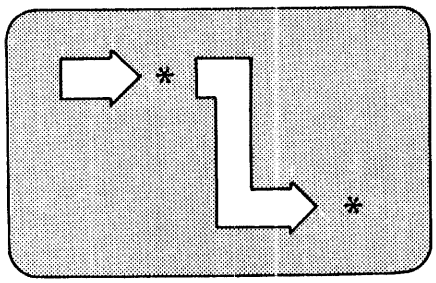
Figure 40. Cursor Control [10819]





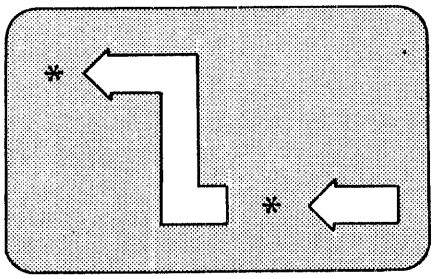
B Backspace Key

Each time this key is pressed, the cursor moves one position to the left, unless it is already in the leftmost position, in which case it moves to the rightmost position of the line above.



A Tabulator Left-to-Right

If the key is held down, the cursor skips rightwards to the first character position (*) of the first unprotected field it encounters, then scans all first character positions of unprotected fields line by line in a left-to-right top-to-bottom movement. On reaching the bottom right-hand corner of the screen, it wraps to the leftmost character of the topmost unprotected field.

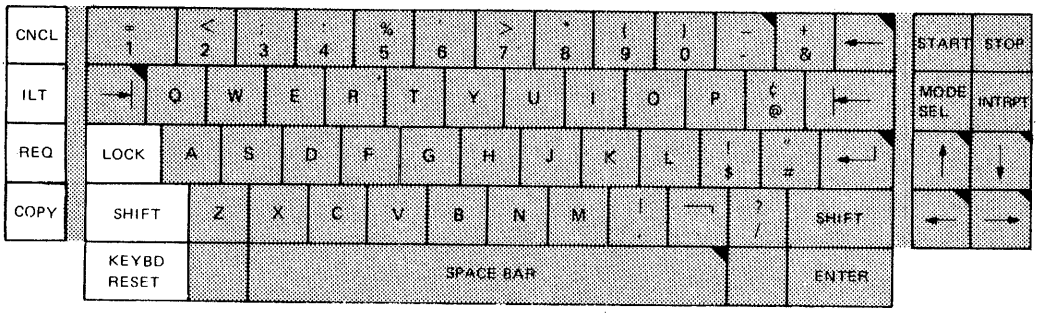


C Tabulator Right-to-Left

The current position of the cursor affects the operation of the back-tabulator key. When the cursor is in an input field at a location other than the first character location, the backtab key repositions it to the first character position in the field. When the cursor is in a protected field, or at the first character position of an input field, the backtab key repositions it to the first character position of the first input field to the left of the present field. It is not a typamatic key.

Backspace and Tabulator Keys

Figure 41. Backspace and Tabulator Keys [10820]



Cancel

If the CNCL key is pressed when the screen is under control of the operating system and a message has been keyed in, the display disappears from the screen. The message is transferred to main storage and an attention interruption is requested.

If CNCL is pressed during manual operations such as alter/display, the display disappears from the screen and control of the screen is returned to the operating system.

Copy

The COPY key can only be used when the 5213 printer (the console printer) is attached to the system and when manual operations are on the screen.

When the COPY key is pressed, the console printer makes a copy of the display on the screen. Only the first 12 lines (and not the machine status area) are copied. During copying, the keyboard (except for the function keys) locks.

In-line Test

Pressing the ILT (in-line test) key causes the repertoire of in-line tests to appear on the screen for selection by the customer engineer. The operating system message (if any) is stored. The ILT key has no function when manual operations are displayed.

Lock

Pressing the shift LOCK key holds the shift keys down. The shift lock is released when either of the two shift keys is pressed.

Request

The REQ key is only effective when the screen is under control of the operating system, not during manual operations. When it is pressed, an attention interruption is generated, usually for the operating system to perform an emergency clearing function.

Shift

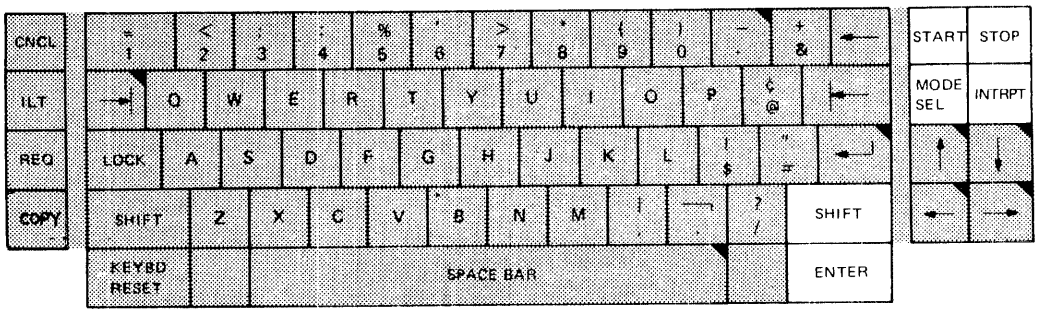
There are two SHIFT keys for use with those alphameric keys which are marked with two characters. When a SHIFT key is pressed together with one of these alphameric keys, the upper character is effective. When the alphameric key is pressed without a SHIFT key, the lower character is effective.

Keyboard Reset

Pressing the KEYBD RESET key restores the use of the keyboard to the operator, after it has been inhibited. If the keyboard is locked, the KEYBD RESET key has no function.

Function Keys

Figure 42. Function Keys (Left-hand Side of Keyboard) [10821]



Start

When the system is in the stopped state, pressing the START key starts the MIP, thus ending the stopped state. The START key is ineffective if the system has a hardstop error condition.

Stop

When the STOP key is pressed, the system stops but not before all instructions currently in progress are completed, and all pending interruptions not masked off are serviced.

Shift

The SHIFT keys are used with those alphameric keys which are marked with two characters. When a SHIFT key is pressed together with one of these alphameric keys, the upper character is effective. When the alphameric key is pressed without the shift key, the lower character is effective.

Mode Select

Pressing the MODE SEL key causes the current message on the screen (if any) to be stored and the repertoire of manual modes to be displayed. The MODE SEL key cannot be used to stop or start the machine.

Pressing the key does not affect any programs running, but if the console printer is working it will stop: the console will appear busy to the operating system.

Interrupt

When the INTRPT key is pressed, an external interruption is generated. The interruption is interpreted solely by the program.

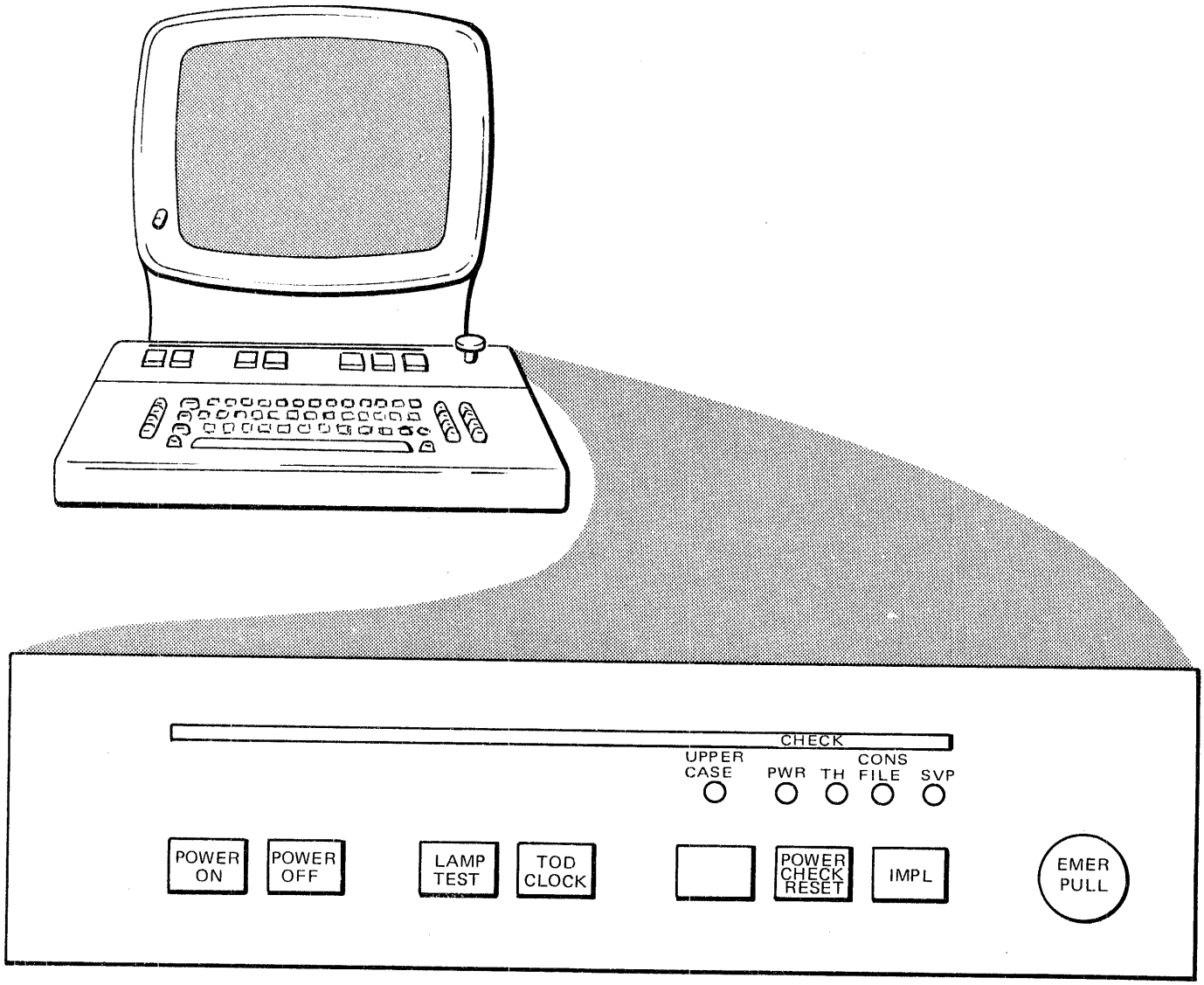
Enter

When the ENTER key is pressed, keyed-in data enters the system and is available to the program. Before the ENTER key is pressed, any keyed-in data can still be changed by the operator.

Function Keys

Figure 43. Function Keys (Right-hand Side of Keyboard) [10822]

The control panel on the operator console keyboard houses a number of switches, keys, and lights (see Figures 45, 46 and 47). The keys are used for basic tasks such as making the system operational. The lights alert the operator to check conditions or upper case mode.



Lights
Keys and Switches

Control Panel

Figure 44. Control Panel [10823]

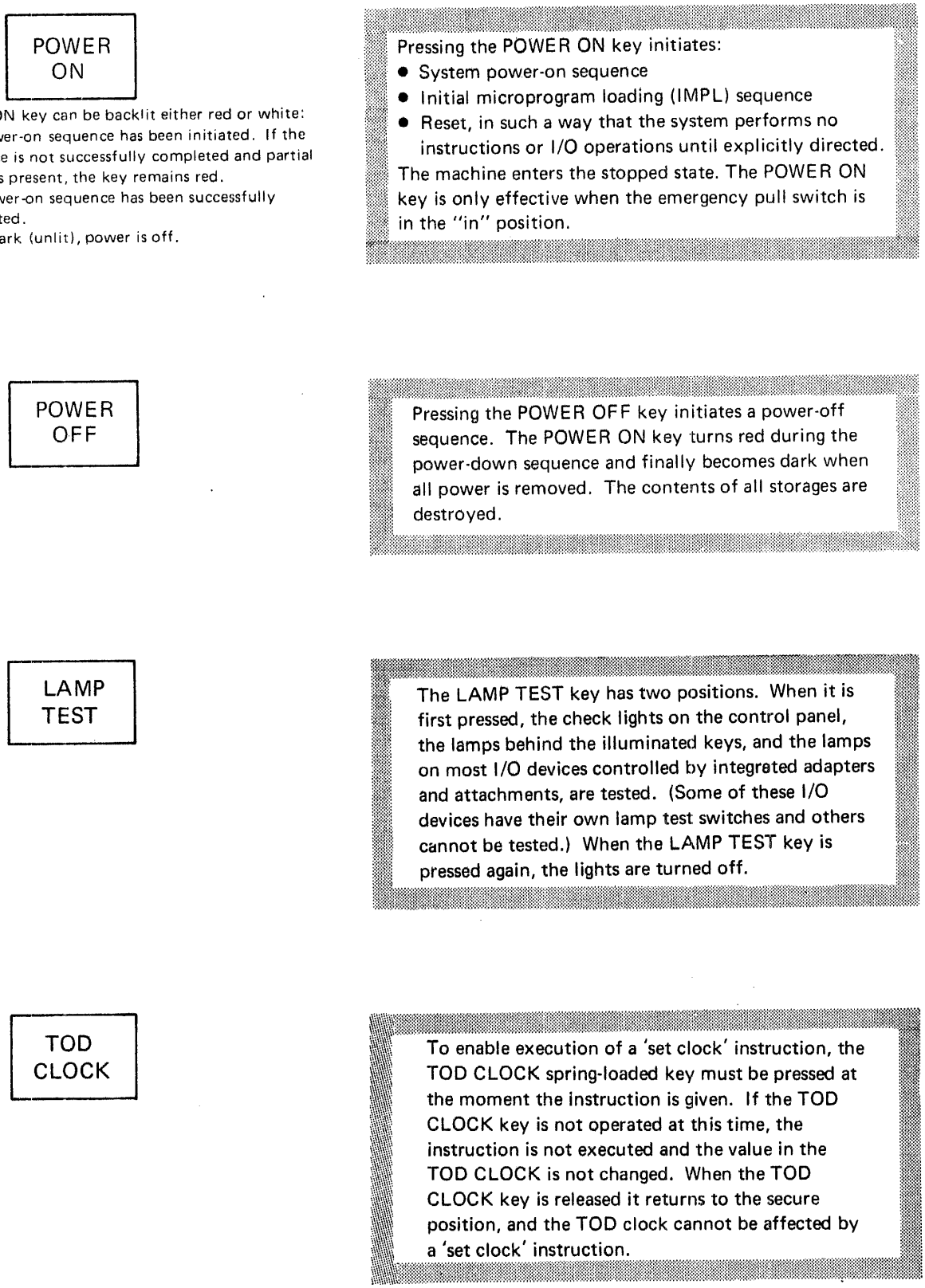
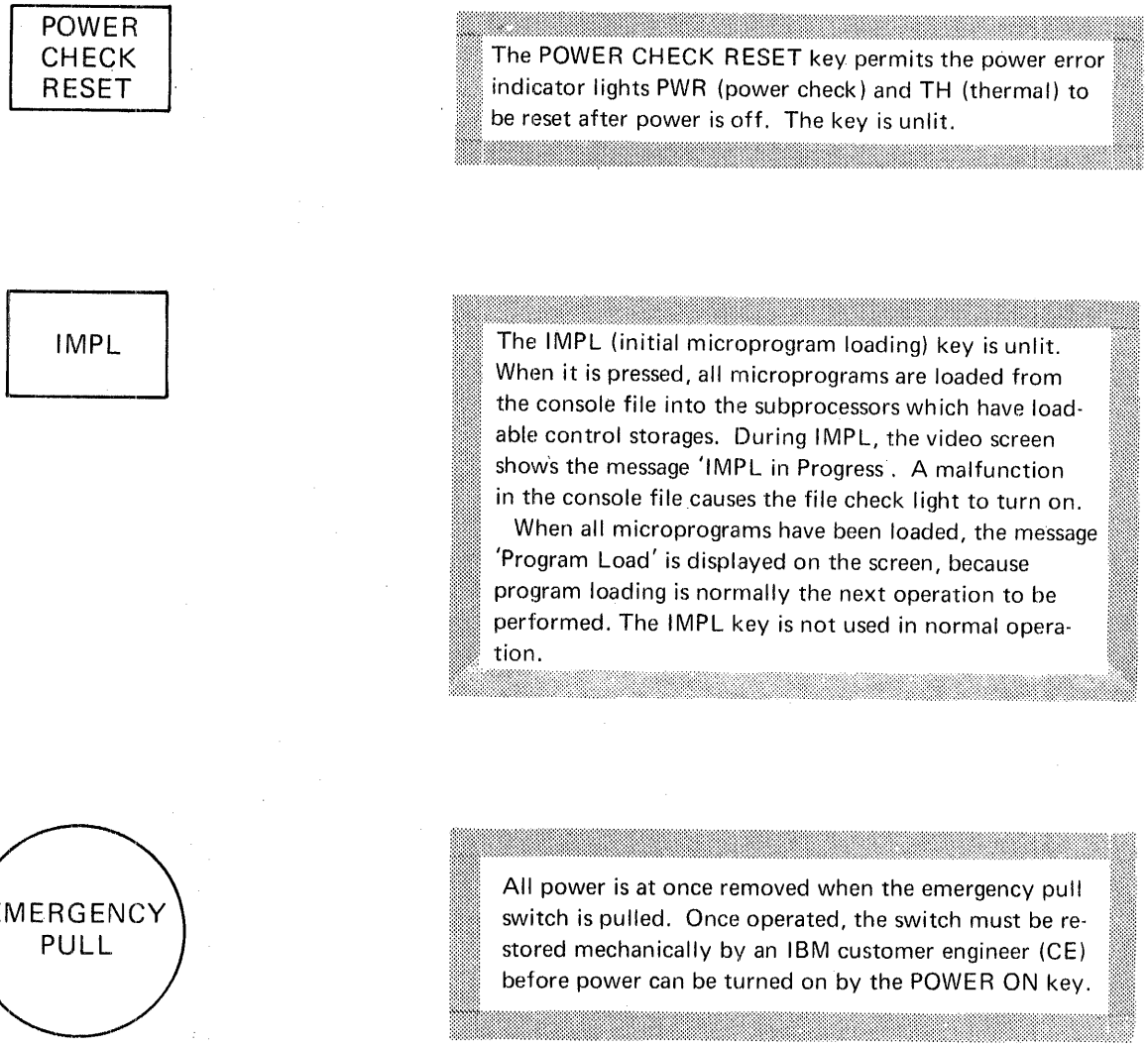


Figure 45. Control Panel Keys [10824]



Control Panel Keys and Switch

Figure 46. Control Panel Keys and Switch [10825]

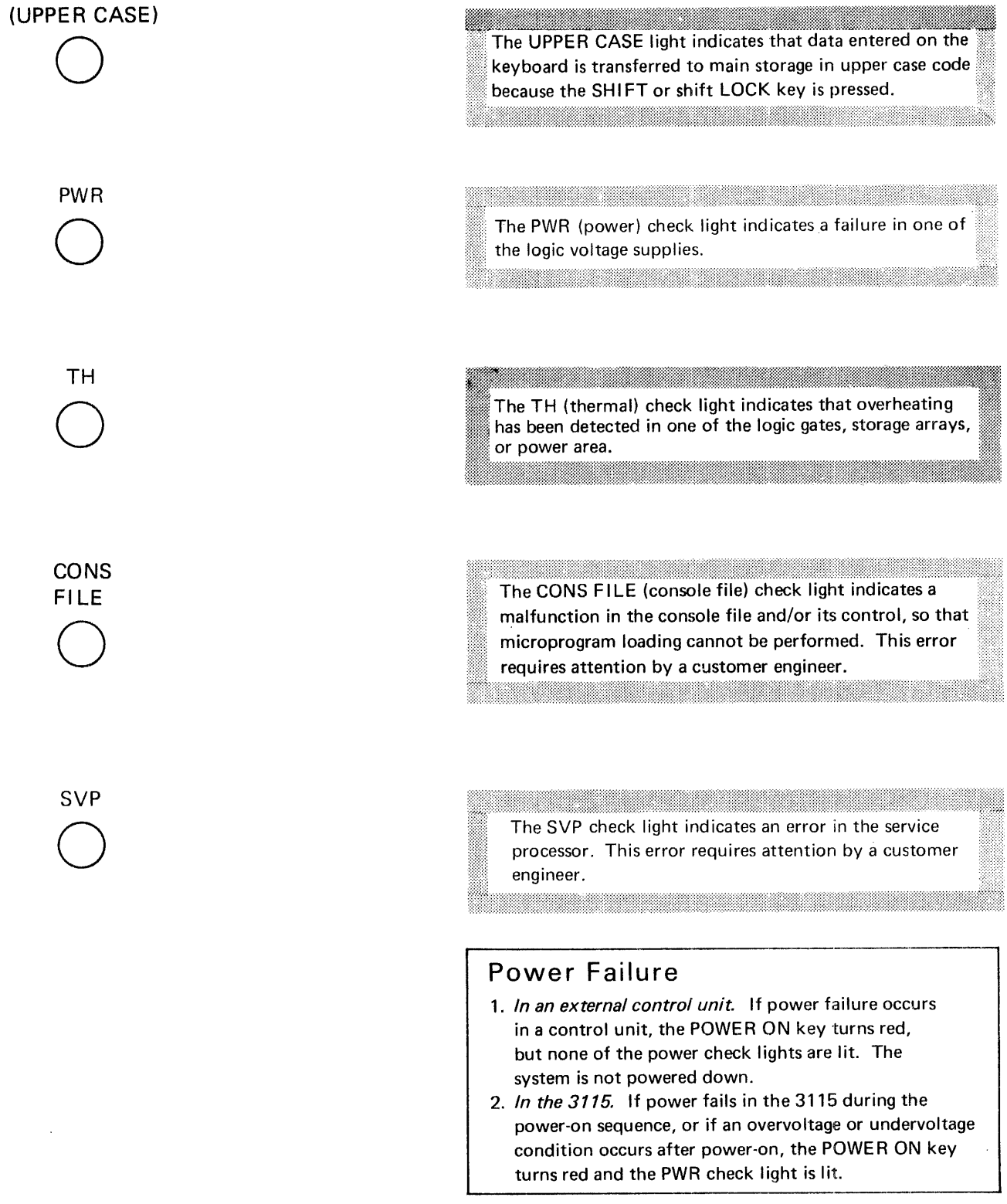
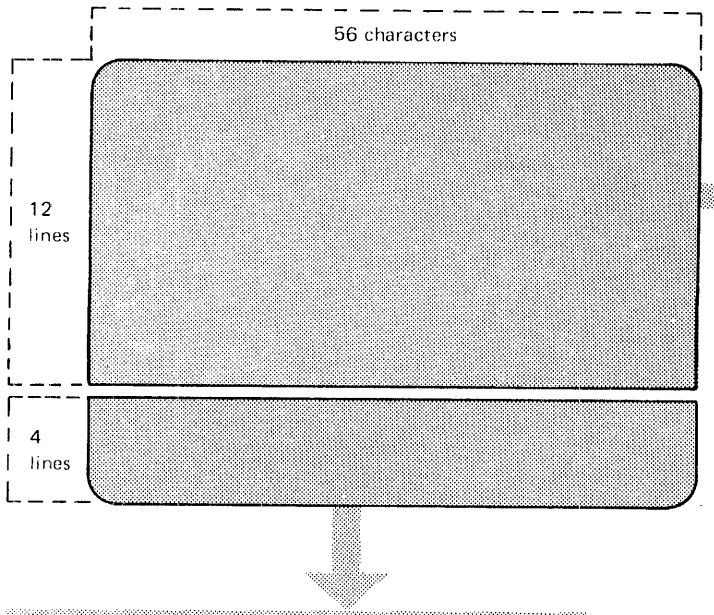


Figure 47. Control Panel Lights [10826]

The Model 115's video display:

- Consists of a 15-inch video monitor attached to the service processor.
- Is mounted on a separate table and rotatable by 180°
- Displays numeric characters, upper case alphabetic characters, and special symbols.
- Is equipped with manual intensity adjustment.
- Is equipped with a program-controlled audible alarm, which alerts the operator to messages requiring attention.

Display Format



System Output Area

This area of the screen is used for displaying messages from the operating system during normal operation. During manual operations, it is used for displaying and selecting operating modes. If the operator is allowed to proceed he uses this area for his response. The cursor marks the beginning of the field assigned to him.

Machine Status Display

This area of the screen permanently displays the machine status.

Video Display

Figure 48. Video Display [10827]

MODE SELECTION

The operator can place the Model 115 into any of the following modes:

- System reset
- Address compare
- Program load
- Interval timer
- Check control
- Storage dump
- ICA line modes
- Alter/display
  - General registers
  - Floating point
  - Current PSW
  - Protection key
  - Main storage real
  - Main storage virtual
  - Control registers
- Instruction step
- Restart
- Maintenance
- Store status
- Save usage counters.

To specify a mode, the operator must first press the MODE SEL key to bring the mode selection display to the video screen. This action does not affect the condition of the machine, which continues in its current state (running, or in the stopped state).

Pressing the MODE SEL key causes the following actions:

1. The last video screen message from the operating system is stored for later use.
2. The mode selection display (Figure 49) appears on the screen, with the cursor positioned at 'Mode Specification'.

The mode selection display lists the operating modes in which the Model 115 can be run. Against each mode listed is a selector character (R, C, L, T, K, D, E, A, I, P, M, S or U) which the operator keys in to set the mode of his choice; for instance 'C' for address compare mode or 'I' for instruction step mode.

When the operator has keyed in the selector character he must press the ENTER key, which will cause a new display, defining the selected mode, to appear. The operator can now expand his specification by, for example, keying in a main storage address or defining registers for display. After he has again pressed the ENTER key, the Model 115 is in the desired mode.

Note: Experienced operators may key *all* specifications for a particular mode direct into the mode selection display. This *fast selection* is described separately for each mode in the following paragraphs.

Mode Selection Errors

Every keyed-in specification is checked for validity as soon as the operator presses the ENTER key. If the first character keyed in is not one shown in the mode selection display, the message 'Invalid Character' appears, and the mode selection display stays on the screen. The cursor marks the error spot. If no character was entered, or fast selection was attempted but the keyboard input was incomplete, the message 'Incomplete Entry' appears.

OPERATING MODES

The following paragraphs describe the available operating modes. Refer to the mode displays shown in Figure 49.

System Reset (R)

When the mode selection display is on the video screen, the operator can obtain the system reset display by keying in the selector character 'R' against 'Mode Specification' on the screen, then pressing the ENTER key. The mode selection display will disappear, and be replaced by the system reset display (see Figure 49). The operator can now specify a normal reset or a clear reset by keying in selector character 'N' or 'C' respectively.

Normal and Clear Resets

If the operator enters selector character 'N', only the CPU and the channels are reset. The contents of the general registers, control registers, floating point registers, main storage, and the current PSW are not changed but the parity in all registers is made valid.

If the operator enters selector character 'C', the entire main storage (including protection keys), general registers, floating point registers and the PSW are reset to zero with valid parity. All timers, except the time of day clock, are reset. The channels and the CPU are reset and the control registers are initialized.

If no errors have been made, the specified reset operation occurs when the ENTER key is pressed. At this time the current CPU instruction (if any) is terminated, pending interruptions or machine check conditions are cleared, and the CPU stops.

The system reset display remains on the screen, and subsequently the message 'Reset Complete' appears. If the operator now presses the START key, the Model 115 starts but the display is not removed. To release the screen to the operating system, the CNCL key must be pressed.

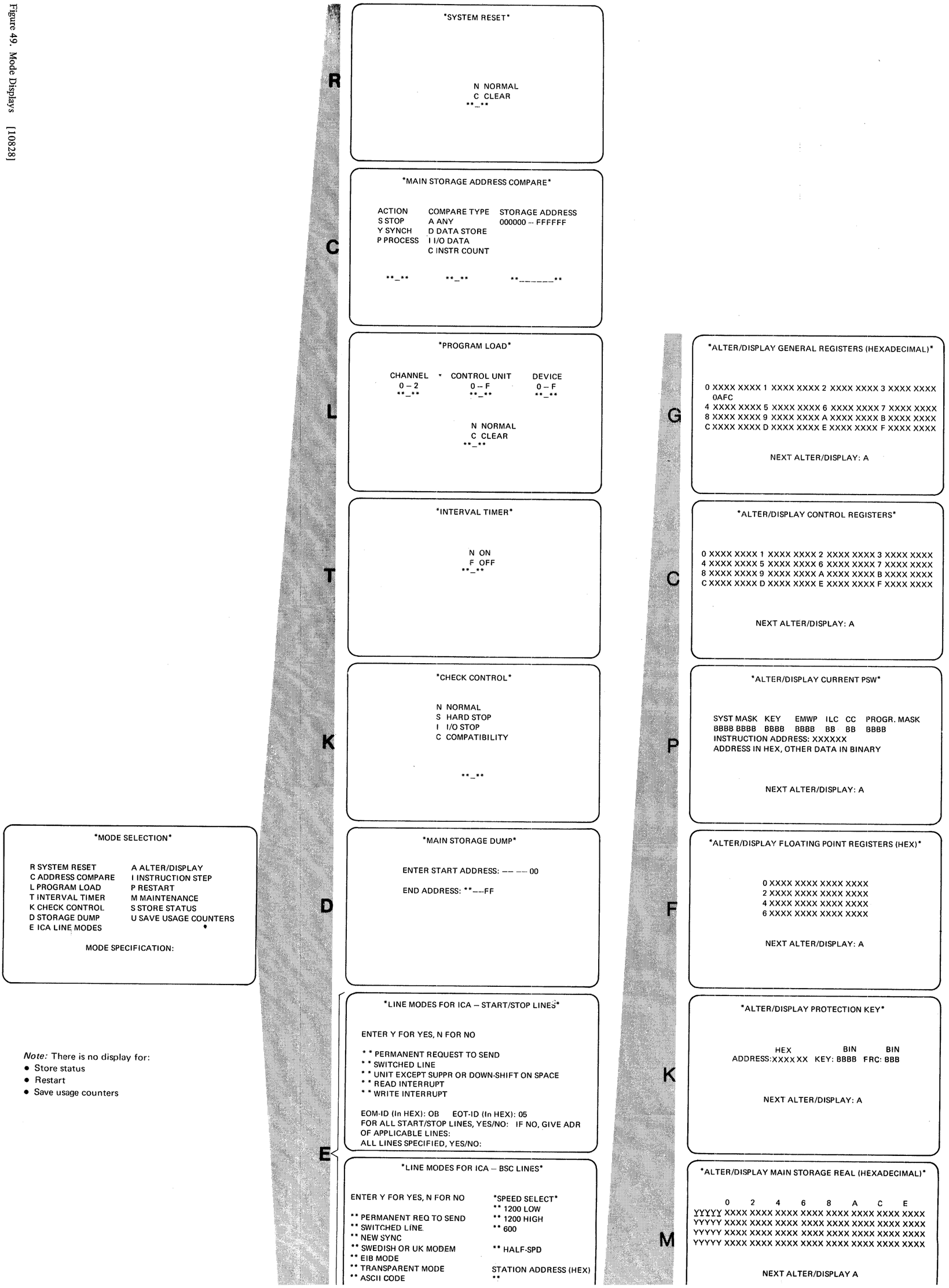
Fast Selection

For fast selection, the operator can enter 'RN' or 'RC' direct into the mode selection display.

Address Compare (C)

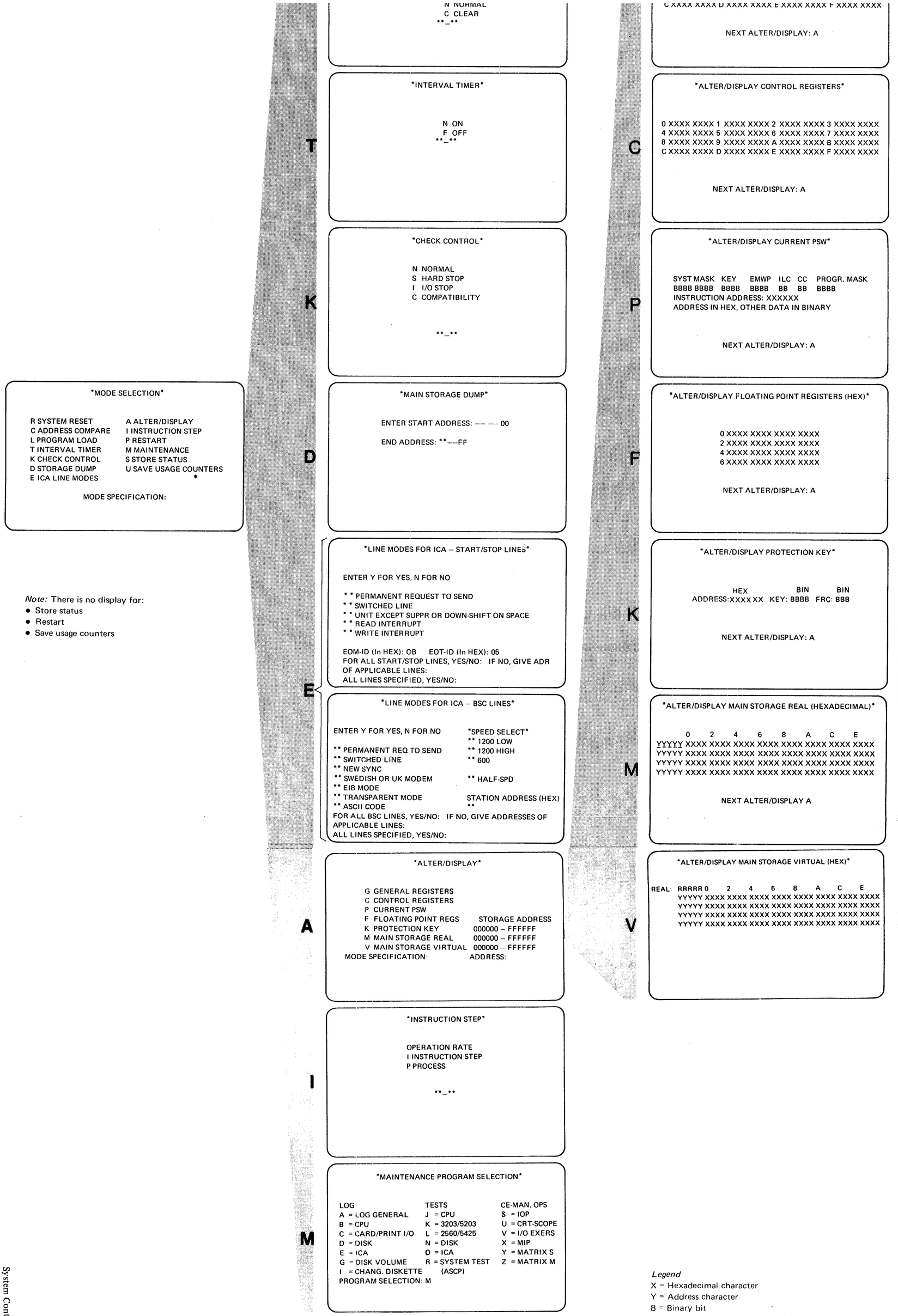
By keying selector character 'C' into the mode selection display and pressing ENTER, the operator brings the main storage address compare display (see Figure 49) onto the screen. The operator must now key in three parameters; the action to be performed, the compare type, and the storage address.

Figure 49. Mode Displays [10828]



Note: There is no display for:

- Store status
- Restart
- Save usage counters



Note: There is no display for:
- Store status
- Restart
- Save usage counters

Legend
X = Hexadecimal character
Y = Address character
B = Binary bit

Mode Displays

Action

The operator must first key in, under the 'Action' heading, one of three code letters which represent the type of action to be performed.

1. *Stop Action (code 'S')* means that the Model 115 will stop when a match with the search address is detected in the conditions specified here under 'Compare Type' (see "Compare Type" below).
2. *Sync Action (code 'Y')* means that the Model 115 will not stop when the address match occurs, but that a synchronization pulse is issued. Processing continues.
3. *Process Action (code 'P')* means that the address compare mode is turned off. If the Model 115 is in the stopped state when 'P' is entered, it remains stopped.

Compare Type

After specifying the type of action to be performed, the operator must next key in one of four code letters. Each letter represents a type of comparison which can be performed.

1. *Any (code 'A')* means that whenever an address is referred to, regardless of the operation, it is compared with the search address.
2. *Data Store (code 'D')* means that only addresses used by the CPU to store data into main storage are compared with the search address. Fetch operations are ignored.
3. *I/O Data (code 'I')* means that only addresses used in transferring data to and from input/output devices are compared with the search address.
4. *Instruction Count (code 'C')* means that only addresses used by the 3115 to fetch instructions are compared with the search address.

Storage Address

The storage address is the last piece of information that the operator must key into the main storage address compare display. The address which is to be the subject of the compare operation must be keyed in beneath the 'Storage Address' legend on the screen, with all leading zeros.

Entering the Specification

When the operator presses the ENTER key, the main storage address compare display disappears from the screen. The specifications that were keyed in are, however, displayed in the machine status area (see Figure 50) as a reminder that address compare mode is set.

Specification Errors

The following messages appear on the screen if the operator has made an error in his keyed-in specification.

Invalid Character: The 'Invalid Character' message appears if an incorrect selector character or non-hexadecimal character has been entered.

Invalid Address: The 'Invalid Address' message appears if an address exceeding the installed storage is specified.

Fast Selection

For fast selection, the operator can key address compare mode direct into the mode selection display. For example, entry 'CSI005FA0' means 'compare and stop during I/O data transfer when address 005FA0 comes up'.

Program Load (L)

When the mode selection display is on the video screen and the operator enters selector character 'L' against 'Mode Specification', the screen picture changes to the program load display (see Figure 49). If initial program loading was performed after power on, the addresses of the channel, control unit, and device originally specified are shown within the program load display.

If the same load device is to be used, the operator should press the ENTER key. If a different device is to be used, the address of the desired channel, control unit, and device must be entered in the correct order.

Fast Selection

For fast selection, the operator can key a program load specification direct into the mode selection display. For example, entry 'L09CN' means 'load from device 09C in normal fashion'.

Location 80 Timer (T)

When the mode selection display is on the video screen and the operator enters selector character 'T' against 'Mode Specification', the screen picture changes to the location 80 timer display (see Figure 49). The current state of the location 80 timer is shown in the machine status area (see Figure 50). The operator therefore knows which character will cause a change. Any new timer state is shown in the machine status area.

Fast Selection

For fast selection, the operator can enter 'TN' or 'TF' direct into the mode selection display to specify interval timer on or off.

Check Control (K)

When the mode selection display is on the video screen and the operator enters selector character 'K' against 'Mode Specification', the screen picture changes to the check control display (see Figure 49). The current check control mode is shown in the machine status area (see Figure 50): if no check control mode has yet been specified, this area will show the check control status as 'Normal', which means that check control conditions are handled as specified by the mask bit in control register 14. The operator can, however, overrule this register by entering one of four code

letters, which represent the following four modes listed in the check control display.

1. *Normal (Code 'N')* turns off any previously-selected check control mode and returns control to the mask bits in control register 14 (see Figure 23).
2. *Hard Stop (Code 'S')* causes the machine to enter the check stop state when any type (hard or soft) of machine check condition occurs. No machine-check interruption code is stored, no limited channel logout is initiated, no internal log is recorded on the console file, and no automatic microprogram reloading is performed for the affected subprocessor.

   During the check stop state, the START key and the restart mode are ineffective. Initial program loading or system reset are the only means of recovery.
3. *I/O Stop (Code 'I')* causes the machine to enter check stop state after a limited channel logout has been stored. Limited channel logouts are generated by a channel data check, channel control check, or interface control check.
4. *Compatibility (Code 'C')* causes the 3115 to enter the check stop state after a limited channel logout or a machine-check interruption has occurred and the values of registers, timers, and so on have been transferred to the assigned main storage positions.

   Note: Compatibility mode must be set before a System/360 program is run.

When one of the listed modes has been correctly entered, the screen display disappears and the machine status area shows the mode entered. A mode check control remains in effect until turned off by the entry 'N' (normal).

Fast Selection

For fast selection, the operator can enter KN, KS, KI or KC direct into the mode selection display.

Storage Dump (D)

The dump facility provides a non-destructive readout and printout of any main storage area (up to 64K bytes at a time) without any software support. The dump can be performed at any time, and the (dumped) program can continue as soon as dumping is completed (no IPL or restart is required).

For dumping, the character 'D' must be typed into the mode selection display, then the ENTER key must be pressed. The operator may then type in start and end addresses of his choice within the prescribed limitations (see Figure 49). The low-order halfword of the start address is limited (preselected zeros) to ensure proper print format. The end address is limited to a 64K range. The operator need only enter two hexadecimal digits because the two asterisks automatically assume the value of the start address digits above them. If more than 64K bytes are to be dumped, the operation must be repeated (with new start and end addresses).

Dumping is initiated as soon as the operator presses the ENTER key, provided no operator errors have been made and the line printer is ready. During dumping all the function keys are operational. This means that the operator can stop dumping at any time by pressing the MODE SEL, CNCL, or START key. If a function key is pressed, the message 'Dump Cancelled' appears on the screen and subsequently, the pressed key takes effect. The MIP is stopped during the dump process (just as if the operator had pressed the STOP key).

Dumping ends automatically when either the selected dump range has been printed or the upper boundary of main storage (real) has been reached. Accordingly, either the message 'Dump Complete' or 'Storage End' appears in the dump display on the screen. The machine is in stopped state at this time. The operator may then dump another storage area or continue with the program by pressing the START key, after pressing the CNCL key to remove the dump display from the screen.

Errors

If the line printer is not ready, the message 'Printer Not Ready' appears on the screen as soon as the operator presses the ENTER key. If the start address is greater then the real storage size, the message 'storage end' appears and no action occurs (the dump facility does not wrap). Invalid characters (non-hexadecimal digits) or incomplete entries are marked as such.

Note: If a log operation coincides with a dump demand, the message 'Press Cancel' appears. The operator should then press the CNCL key and will see 'Log In Progress' displayed on the screen in the machine status area. Dumping can be repeated as soon as the log message disappears.

Fast Selection

No fast selection code is provided for storage dumping.

ICA Line Mode (E)

ICA line mode displays are only available if the Model 115 has an integrated communications adpater installed. Two displays may be obtained, one for start/stop lines, and one for binary synchronous communications (BSC) lines.

Start/Stop Lines

To obtain the start/stop lines (or BSC lines) display, the operator must enter selector character 'E' against 'Mode Specification' on the mode selection display, the operator may type in 'Y' or 'N' (yes or no) as applicable against the first five legends on the start/stop lines display (refer to Figure 49). Most of the specifications have a dual meaning, the second of which is implied. For example, answering 'N' to 'Permanent Request To Send' means not-permanent request to send, that is, half-duplex operation. Answering 'N' to 'Switched Line' means leased line. The operator

must, therefore have some knowledge of teleprocessing to complete the specification successfully.

The end-of-message and end-of-transmission identifiers ('EOM-ID' and 'EOT-ID') have pre-selected (default) values and may be ignored if there are no world trade leased telegraph lines attached to the system. To ignore the identifiers, the operator moves the cursor to the next item by pressing the new line key. If there are world trade leased telegraph lines attached, the default values may be used or one or both may be changed. Care must be taken when entering new values for EOM or EOT because these apply always to the entire line group (not to an individual line). For example, there could be two line groups, where group 1 covers line address 20 to line address 27, and group 2 covers 28 to 2F. EOM and EOT may be different for each group but not different for lines, within a group. In addition, the operator must select a character in downshift mode as identifier; upshift characters are not recognized.

The operator must next enter 'Y' or 'N' against the legend 'For All Start/Stop Lines'. If he enters 'Y', he should then press the new line key to skip the next item (which is not applicable) and go to the last line.

If the lines are not all start/stop lines, the operator must enter 'N', and the hexadecimal addresses of the lines to which the modes are to apply. The line addresses may be entered in any sequence.

The operator must now enter 'Y' or 'N' against the last legend on the screen – 'All Lines Specified'. If he keys in 'Y', the start/stop lines display is replaced on the screen by the BSC lines display. If he keys in 'N', the specifications already keyed into the display disappear as soon as the ENTER key is pressed. These specifications are stored and the operator can continue to key in specifications for any remaining start/stop lines. When the modes have been specified for all start/stop lines, the operator can enter 'Y' against the last legend, which will cause the ending message or the BSC picture to appear when the ENTER key is pressed.

Errors: Errors such as specifying switched line although a leased line is installed, or entering an upshift character as EOM or EOT identifier, are not rejected.

If the operator enters other than 'N' or 'Y' or enters non-hexadecimal values, the specification is rejected and the 'Invalid Character' message appears on the screen. Entering addresses other than those from 20 to 2F causes the 'Invalid Line Number' message to appear. If a line group is not installed but a valid address for that group is entered, no error message is displayed. Whenever errors can be corrected by the operator, the display remains on the screen and the cursor marks the first error.

If the operator enters 'N' against 'For All Start/Stop Lines' but gives no line addresses or not enough line addresses, no error results because the system assumes the default values. Entering 'N' against 'For All Start/Stop Lines', then giving no applicable line address is equivalent to a cancellation of the entered specifications. For further information on the default values, see the description of the 'set line mode' command for the appropriate line control procedure in the "Teleprocessing Characteristics" chapter.

Note: To avoid errors in EOM or EOT specifications, operators are recommended to change or enter values only when the last line of the line group has been specified. This is because the last EOM or EOT specification always overwrites any previous one and thus becomes valid for the group.

BSC Lines

The BSC lines display appears as soon as all start/stop lines have been specified or, if there are no start/stop lines, the BSC lines display is the first (and only) display to appear when the operator specifies ICA line modes. The operator specifies modes on the screen in a similar way to that already described for start/stop lines. Again, most specifications have a dual function. For example, entering 'N' against 'Switched Line' means leased line; entering 'N' against 'ASCII Code' means EBCDIC; entering 'N' against 'Swedish Or UK Modem' means all other.

The 'Speed Select' specification applies to the internal clock. The 1200 (bits per second) speed can be specified as high or low to accommodate 2400/1200 and 1200/600 type modems. Such modems require the 'data signaling rate selector' interface line to be either on or off depending on whether 1200 is the higher or lower of the two modem speeds. The 'Half-Spd' specification is for self-clocked modems with two speeds. A 'Y' entered against 'Half-Spd' selects the lower speed.

The 'Station Address' is specified only when a line is to operate as a tributary station in a multipoint network. A polling or selection address may be given in the form of two hexadecimal digits.

The operator must next enter 'Y' or 'N' against the legend 'For All BSC Lines'. If he keys in 'Y', he should skip the next item on the screen. If he keys in 'N', he must also enter the addresses of all the lines for which the specifications are intended. The operator must now enter 'Y' or 'N' against the last legend on the screen – 'All Lines Specified'. Entering 'Y' brings the ending message to the screen. Entering 'N' causes all previously entered specifications to disappear from the screen (they are stored) so that the operator can continue to specify the modes for any remaining lines.

Errors: Errors in the operator's specification, such as specifying switched line where a leased line is installed or specifying '1200 High' where '1200 Low' is required, are not rejected.

Errors such as using non-hexadecimal digits or characters other than 'N' or 'Y', result in rejection of the specification; the 'Invalid Character' message appears on the screen.

Obvious technical errors are rejected and the message 'exclusivity error' is displayed on the screen. The following specifications are mutually exclusive:

'Switched Line' and 'New Sync'

'ASCII Code' and 'Transparent Mode'

More than one speed selection.

If the operator specifies a line address other than 30 to 34, or 36, the specification is rejected and the 'Invalid Line Number' message appears on the screen. Note that line address 35 is invalid.

The applicable error message appears on the screen as soon as the operator presses the ENTER key. The BSC lines display remains on the screen and the operator can correct any specification errors; the position of the cursor indicates the first detected error.

If the operator specifies line addresses for lines which are not installed, no error message is displayed. Similarly, if the operator keys in 'N' against the 'For All BSC Lines' legend, but gives no line addresses or not enough line addresses, no error results because the system assumes the default values. Giving no addresses is equivalent to a cancellation of the entered specifications.

Ending Message

The ending message appears on the screen when the operator presses the ENTER key after entering 'Y' against the 'All Lines Specified' legend in the last (possibly the only) line mode display. The ending message is 'Line Modes Become Operational With IMPL Or Power-On'.

The operator may either press the IMPL key (to make the line modes immediately effective) or wait until the next time that power-on (which includes automatic IMPL) is performed. The operator may then proceed as is convenient. To remove the ending message from the screen, he may press the CNCL, MODE SEL or IMPL key.

The specified line modes are permanently stored when the operator presses the ENTER key, so if he decides to wait for the next power-on, rather than making the line modes immediately effective, there is no disadvantage. The operator may change the specified line modes at any time, but it is not possible to recall the previously-entered specifications onto the screen.

Programming Note

If the teleprocessing system uses the set line mode commands, such commands have priority over any manually-entered specifications. However, line mode commands are not permanently stored and are, therefore, effective only as long as power is on.

Fast Selection

No fast selection code is provided for the ICA line mode displays. This is because the line modes need be specified only once, at installation, and then only if the teleprocessing system does not use set line mode commands.

Alter/Display (A)

When the mode selection display is on the video screen and an 'A' is entered against 'Mode Specification', the screen picture changes to the alter/display repertoire (see Figure 49) and the program stops. This repertoire lists the facilities that can be displayed and altered. Against each mode listed is a selector character (G, F, P, C, K or M) which the operator may key in to display the information of his choice; for example, 'G' for general registers or 'K' for protection key.

Notes:

1. If the operator wishes to change the screen picture from one of the displays in the alter/display repertoire to another alter/display operation, he can enter the relevant selector character against the legend 'Next Alter/Display: A'; otherwise he presses the MODE SEL key once for the alter/display repertoire, or twice for the mode selection display.
2. The operator may alter data on any of the subdisplays within the alter/display repertoire, by first moving the cursor under any hexadecimal digit. He can then type in new data which will appear under the current contents. If he next presses the ENTER key, the new data replaces the old. The operator may press the ENTER key after keying in each digit, or after keying in all digits he wishes to change. After he has pressed the ENTER key, the subdisplay remains on the screen.

The following text describes the facilities that can be displayed via the alter/display repertoire.

General Registers

If the operator keys selector character 'G' into the alter/display repertoire (or has used fast selection to key 'AG' into the mode selection display), the general registers are displayed on the screen (see Figure 49). All sixteen general registers are shown on the screen at the same time. The contents of each register are displayed as eight hexadecimal characters (each representing four bits), grouped in halfword format.

To change one or more hexadecimal characters, the operator must position the cursor under the first character to be altered and key in the desired data. When he presses the ENTER key, the new data replaces the old on the screen, and is stored in the register. The display remains on the screen and the cursor is now at 'Next Alter/Display: A'. The character 'A' is preselected so that further information can be displayed by entering F (for floating point) or P (for PSW).

If the operator wishes to display another facility but does not remember the selector character, he presses the MODE

SEL key, which brings the alter/display repertoire (*not* the mode selection display) back to the screen. If he wants the mode selection display, he must press the MODE SEL key again.

If the operator wishes to resume operation, he can do so by pressing the START key. The system starts to process instructions again, but the display remains on the screen. If the operator then presses the STOP key, the system stops and the screen displays the current contents of the general registers.

Note: After an alteration, the system does not start until the operator presses the START key.

Selection Errors: If the operator enters an unspecified hexadecimal character, no change takes place and the legend 'Invalid Character' appears on the screen.

Floating Point Registers

If the operator wishes to display the contents of the floating point registers on the video screen (see Figure 49), he should enter selector character 'F' into the alter/display repertoire. He can also display the floating point registers by keying in 'A' at the end of the legend 'Next Alter/Display: A' in any subdisplay of the alter/display repertoire, or by keying 'AF' direct into the mode selection display (fast selection).

All eight floating point registers are displayed at the same time. The contents of each register are displayed as eight hexadecimal characters (each representing four bits), grouped in halfword format.

Current PSW

To display the current PSW on the screen (see Figure 49), the operator should enter selector character 'P' either into the alter/display repertoire or, if a subdisplay of this repertoire is on the screen, against the legend 'Next Alter/Display: A'. He can also bring the PSW to the screen by keying 'AP' direct into the mode selection display (fast selection). Entering the selector character causes the machine to stop and the current PSW to be displayed.

The PSW display is in binary notation, except for the instruction address which is in hexadecimal.

Control Registers

To display the contents of the control registers on the screen (see Figure 49), the operator should enter selector character 'C' either into the alter/display repertoire or, if a subdisplay of this repertoire is on the screen, against the legend 'Next Alter/Display: A'. He can also bring the control registers to the screen by keying 'AC' direct into the mode selection display.

All sixteen control registers appear on the screen at the same time. The contents of each register are displayed as eight hexadecimal characters (each representing four bits), grouped in halfword format. The procedure for altering the contents of control registers is the same as previously described under "General Registers".

Protection Key

To display a protection key on the screen (see Figure 49), the operator must enter selector character 'K' either into the alter/display repertoire or, if any subdisplay within this repertoire is on the screen, against 'Next Alter/Display: A'. The operator must also specify a main storage address.

For fast selection, the operator can key 'AK', followed by the main storage address, direct into the mode selection display.

The protection key is shown as four binary bits immediately to the right of the word 'Key'. The three bits that follow are the reference bit, the change bit, and the protection bit.

Selection Errors: If an address larger than the installed storage is entered, the message 'Invalid Address' appears. If a character other than 0 through F is entered, 'Invalid Character' appears.

Main Storage Real

To display a section of main storage, 32 halfwords at once, on the screen (see Figure 49), the operator must enter selector character 'M' either into the alter/display repertoire or, if any subdisplay within the repertoire is on the screen, against 'Next Alter/Display: A'. The operator must also specify a main storage address. For fast selection he can key 'AM', followed by a main storage address, direct into the mode selection display. The address which the operator keys in is taken as a real address, associated with a portion of real main storage.

The display shows the halfwords in hexadecimal notation. The Y characters, shown in frame M on Figure 49, represent real addresses minus their low-order hexadecimal digits. The low-order hexadecimal digit of the address is shown above each leftmost byte of halfword (0, 2, 4, 6, 8 A, C, E). In this way each halfword can be identified. The address which the operator specified is shown at the top (underlined). If the operator wants to see another portion of real storage, all he needs to enter against the 'Next Alter/Display: A' line is 'M' and a new address.

As previously described, another mnemonic may be entered against the 'Next Alter/Display: A' legend to obtain (for example) the floating point registers display. Mnemonics other than those for alter/display operations will cause the alter/display repertoire to appear with the invalid selection character and the 'Invalid Character' message in it.

If the operator does not remember a mnemonic, he can press the MODE SEL key to obtain the alter/display repertoire. To restart the machine, he must press the START key. To remove the display from the screen, he must press the CNCL key.

Main Storage Virtual

To display 32 main storage halfwords on the screen by using a virtual address (see Figure 49), the operator must enter selector character 'V' either into the alter/display repertoire or, if any subdisplay within the repertoire is on the screen, against 'Next Alter/Display: A'. The operator must also specify virtual main storage address. For fast selection, he can key 'AV', followed by a virtual main storage address, direct into the mode selection display. Pressing the ENTER key will then start the MIP for the purpose of dynamic address translation.

If segment and page are available, the display is the same as the main storage real display previously shown except that the word 'Virtual' replaces 'Real' in the heading. Except for the uppermost address (which is a real address), all others are virtual addresses. The RRRRR address shows the real equivalent of the virtual address underneath. This allows virtual addresses to be seen in relation to the real main storage location.

If the checks performed during dynamic address translation show that either the segment or the page is not available or the operator's specification was invalid, the main storage section is not displayed and one of the following messages appears on the screen:

'Outside Page Table'
'Outside Segment Table'
'Page Entry Invalid'
'Segment Entry Invalid'
'Specification Exception'
'Addressing Exception'

'Outside Page Table': This message means that the address computed from the contents of the segment table points to a location outside the page table.

'Outside Segment Table': This message means that the automatic check against the segment table length in control register 1 revealed that a location outside the segment table would be addressed.

'Page or Segment Entry Invalid': This message means that the desired segment or page is not currently in physical storage.

'Specification Exception': This message means that the page or segment entry does not have zeros in the prescribed bit positions (it is improperly specified).

'Addressing Exception': This message means that the address intended for reference to page or segment entries points to a location outside real main storage.

Operator errors (such as using non-hexadecimal digits) will, of course, produce the 'Invalid Character' or 'Incomplete Entry' message. As usual, the system is stopped when the display is shown. The START key must be pressed to continue processing, the CNCL key must be used to return the screen to the operating system. Alterations are performed as previously described. The 'Next Alter/Display' line can be used to specify another virtual or real address or another facility.

Instruction Step (I)

When the mode selection display is on the video screen and the operator enters selector character 'I' against 'Mode Specification', the screen picture changes to the instruction step display.

If the operator again enters character 'I', the machine stops, the display disappears, and the legend 'I-Step' appears in the machine status area. Instruction step mode is now set, and one instruction will be executed each time the START key is pressed. If the operator selects another mode, such as alter/display, it will be accepted and instruction step mode will remain in effect. Thus, new data can be seen on the screen as soon as each instruction step has been completed. In addition, the machine status area shows the address (and the data at this address) at which the 3115 stopped. This allows detailed tracing at each instruction step.

Instruction step mode is turned off by entering 'P' from the keyboard.

Fast Selection

For fast selecting, the operator can enter 'II' direct into the mode selection display.

Restart (P)

If the mode selection display is on the video screen and the operator enters selector character 'P' against 'Mode Specification', restart mode is set and the screen is at the disposal of the operating system. If the 3115 was in the stopped state, it starts with the program restart PSW. If it was already running, it branches back to the program restart PSW. Restart mode has no screen display.

Note: The restart mode cannot be set if the machine is in the check-stop state.

Maintenance (M)

When the mode selection display is on the video screen and the operator enters selector character 'M' against 'Mode Specification', the screen picture changes to the maintenance repertoire. This repertoire consists of log analysis, micro tests, and CE manual operations. The cursor is positioned next to the preselected 'M' so that any one of the maintenance modes can be selected.

Log Analysis (A–G)

When a parameter 'A' through 'G' is entered into the maintenance display, log information is brought to the screen. Entering A, for instance, causes general log information to be displayed, which informs the operator if any logging occurred, and if so, which part of the system caused it. From this report, the operator can select a

detailed log by keying in one of the five characters 'B' through 'G'. For example, 'B' provides log information for the CPU.

Micro Tests (J–R)

When a parameter 'J' through 'R' is entered into the maintenance display, certain micro tests are performed. If, for example, the log analysis showed error logs on the line printer, the 3203/5203 micro test (K) can be selected to locate the malfunction.

Note: After a micro test has been run, the IMPL key must be pressed to restore the microprograms.

CE Man Ops (S–Z)

CE manual operations are provided for the customer engineer, and can only be run when the CE key is inserted.

Store Status (S)

The store status mode has no display. When the operator enters selector character 'S' into the mode selection display, the status of certain facilities is automatically stored into fixed main storage areas as shown in the following table:

Status	*Stored into Storage Location (decimal)*
CPU timer	216
Clock comparator	224
PSW (current)	256
Floating point registers 0 to 6	352
General registers 0 to F	384
Control registers 0 to F	448

When the ENTER key is pressed, the mode selection display remains on the screen and the message 'Status Stored' appears. From this time on, the system is in the stopped state. The mode specification (that is, the character 'S') disappears and another operation, such as program load, can be specified.

Save Usage Counters (U)

The save usage counters mode has no display. When the operator enters selector character 'U' into the mode selection display, the usage counters of all disk drives are logged on the internal diskette. The 'counter saved' message appears for each counter that is recorded. If an in-line test is in progress on a disk drive, 'Terminate In-Line Test' message appears. The operator may repeat the counter saving after termination of the test. The operator should always carry out the save usage counters operation before switching power off. This preserves the usage figures for the CE, who needs the information for maintenance.

MACHINE STATUS AREA

The machine status area (Figure 50) consists of lines 13, 14, 15, and 16 – the lowest four lines of the screen. These four lines show the state of the machine; for example, whether it is running, stopped, or has a check-stop condition. Any special modes which may have been set, such as instruction step mode or address compare mode, are also shown. The machine status area is not shown when maintenance displays are on the screen. The following paragraphs describe the possible machine status displays.

Line 13

Line 13 shows the state of the 3115, the keyboard, and the console printer, if installed. From left to right, four fields showing the mode of operation and the state of 'KB' (keyboard), 'Cnsl-Prtr' (console printer), and 'Timer' are provided.

Mode Field

The Mode field shows the current mode of operation of the 3115. Any one of the ten following legends can appear.

Sys: The legend 'Sys' (system) is on the screen whenever the system use meter is running. When 'Sys' is not on the screen, the system use meter is not running.

Man: The legend 'Man' (manual) is on the screen whenever the 3115 has been stopped by pressing the STOP key or by certain manual operations (such as alter/display) or during a normal stop (such as occurs in instruction step mode and address compare mode).

Wait: The legend 'Wait' is on the screen whenever the wait state bit in the current PSW is set. 'Wait' does not appear if the wait state bit in the current PSW is off or a PSW looping error has occurred.

Test: The legend 'Test' is on the screen if any of the following conditions applies:

Instruction step mode is set.
Address compare mode is set.
Any check control mode is set.
An in-line test is running.

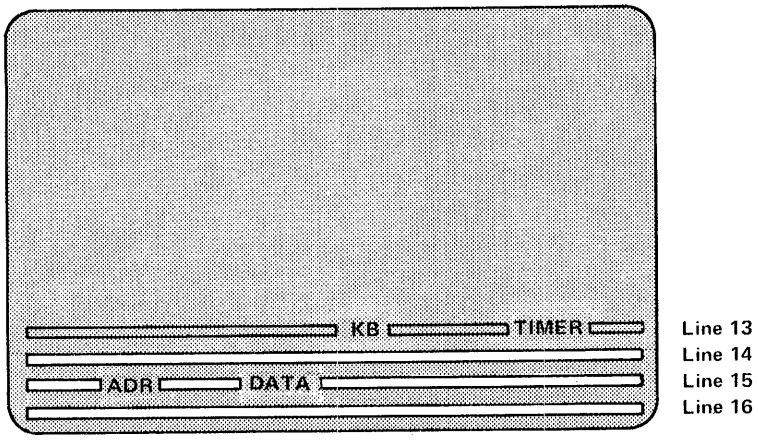
'Test' does not appear for program-initiated tests such as On-Line Tests (OLTs) or the on-line standalone executive program (OLSEP), or program event recording. It is also off during log operations. 'Test' is not affected by the interval timer.

Load: The legend 'Load' appears on the screen as soon as the operator has started the load operation by pressing the ENTER key. 'Load' remains on the screen until a valid PSW is loaded.

Check-Stop: The legend 'Check-Stop' appears on the screen (at the positions otherwise occupied by 'Sys', 'Man', and 'Wait') whenever a check-stop occurs.

PSW-Loop: The legend 'PSW-Loop' appears on the screen (at the positions otherwise occupied by 'Man' and 'Wait') if

Permanent Display



Display Repertoire

Line 13

```
CHECK-STOP                    PROCEED
    PSW-LOOP                  INHIBIT                                  OFF
SYS MAN WAIT TEST LOAD  KB: LOCK      REQ CNSL-PRTR  TIMER: ON
    IPL ERROR
    EC-PSW ERROR
    PSW-ADR ERR
```

Line 14

```
                                      I-COUNT
                                      DATA STORE        SYNC
ADR COMP  REAL  ADR XXXXXX  TYPE: ANY            ACT: STOP  I-STEP
                                      I/O
```

Line 15

```
EC      VIRT                                                  I/O STOP
BC  DAT REAL  ADR XXXXXX  DATA XXXX  CHK-CTL                  HARD STOP
                                                              COMPATIBLE
```

Line 16

(CE Information)

Machine Status Display

Figure 50. Machine Status Display [10829]

a problem occurs in which the program continually loops to the same PSW.

IPL-Error: The legend 'IPL-Error' appears on the screen when the system was unable to load a valid PSW. This condition can occur when the load device is not ready, an invalid address is specified, or an interruption is incorrectly executed. The legend 'IPL-Error' occupies screen positions normally reserved for 'Sys', 'Man', and 'Wait'.

'EC-PSW Error': The legend 'EC-PSW Error' appears on the screen when the load process has ended with an attempt to load a PSW with an invalid EC mode format, and processing cannot continue. The legend 'EC-PSW Error' occupies the screen positions normally reserved for 'Sys', 'Man', and 'Wait'. It indicates that a correct program should be loaded.

'PSW-Adr Err': The legend 'PSW-Adr Err' appears on the screen when the system cannot continue processing because the instruction address in the current PSW is not an address in physical storage. The legend occupies the screen positions normally reserved for 'Sys', 'Man', and 'Wait'. It indicates that a correct program should be loaded.

KB Field

The KB (keyboard) field shows the state of the keyboard. Any one of four legends can appear in this field.

Proceed: The legend 'Proceed' means that the operator can use the keyboard to type in data. All keys are unlocked and will respond.

Inhibit: The legend 'Inhibit' means that the data entry keys are disabled because the operator tried to enter data into a protected area on the screen. When 'Inhibit' is on the screen, the operator can use the KEYBD RESET key to enable the keyboard.

Lock: The legend 'Lock' means that the system has locked all keys capable of interfering with the current operation. The operation may be, for example, a main storage transfer, or a log operation. When the 'Lock' legend is on the screen, the KEYBD RESET key has no function.

Req: The legend 'Req' (request) means that the operator has pressed the REQ key and the request has been accepted. Requests are interpreted by the operating system.

Cnsl-Prtr Field

The Cnsl-Prtr (console printer) field is used when a console printer is installed and the printer's supply of forms is exhausted or its cover is open. The field is also used to indicate console printer errors after a system reset or IMPL operation. The 'Cnsl-Prtr' legend is a request for operator intervention.

Timer Field

The Timer field shows the state of the interval timer at main storage location 80. The legend 'On' or 'Off' appears, depending whether the timer has been enabled or disabled.

Line 14

Line 14 consists of one field, for displaying information on two special modes: address compare and instruction step. When neither of these modes applies, the whole line is blank. When either or both of the modes are selected, the information on the selected special mode appears on the screen.

Adr Comp

When 'Adr Comp' appears on the screen, address compare mode has been set. The following information (described in more detail under "Main Storage Address Compare" earlier in this section) is also shown.

Real: The legend 'Real' indicates that the search address is a real address.

Adr: The search address entered for the address compare operation is displayed after the legend 'Adr' (address).

Type: The legend 'Type' is followed by the indicator 'Any', 'Data Store', 'I-Count', or 'I/O' and shows the type of comparison to be made.

Act: The legend 'Act' (action) is followed by the indicator 'Stop' or 'Sync' and shows the action to be performed when an address match occurs.

I-Step

When the legend 'I-Step' appears on the screen beside 'Mode', instruction step mode has been set.

Line 15

Line 15 provides additional information on the state of the system. From left to right, three fields are shown: the control mode (basic or extended) field; the address and data field; and the check control field.

Control Mode Field

The control mode field shows the current control mode of the system, as follows.

EC and BC: Either of these two legends is on the screen; 'EC' (extended control) whenever bit 12 of the current PSW is set, and 'BC' (basic control) whenever bit 12 of the current PSW is off.

DAT: This indicator is on the screen when the EC mode PSW bit 5 (DAT bit) is set.

Address and Data Field

The Address and Data field shows the address mode, the main storage location of the next instruction, and the associated data, as follows.

Virt: The legend 'Virt' (virtual) means that dynamic address translation (PSW bit 5) was set when the system stopped.

Real: The legend 'Real' means that dynamic address translation (PSW bit 5) was off when the system stopped.

Adr: The 'Adr' (address) field shows the storage address of the instruction to be processed. This address is always the instruction address in the current PSW. When the system is in the check-stop or wait state the address is not shown but it can be brought onto the screen by a display PSW operation.

Data: The 'Data' field shows the halfword stored at the main storage location indicated by the address field. The first byte of this halfword is the op code of the next instruction.

Chk-Ctl Field

The Chk-Ctl (check control) field shows any one of three selectable modes. If the check-control mode is normal, as it is after initialization of control register 14, the Chk-Ctl field is blank.

Hard Stop: The legend 'Hard Stop' means that a check-stop takes place immediately when a machine check occurs.

I/O Stop: The legend 'I/O Stop' means that a check-stop takes place after a limited channel logout is performed.

Compatible: The legend 'Compatible' means that a check-stop takes place after a machine check interruption or a limited channel logout has occurred.

Line 16

Line 16 is reserved for displays and special messages for the customer engineer when special modes, such as logging or in-line tests, are being run.

Usage Metering

The system usage meter is located near the diskette in the CPU main frame. The meter covers all activity in the main storage controller, and in the subprocessors. The system usage meter stops if the CE meter is switched on.

The modes and conditions during which the meter runs are summarized in Figure 51.

I/O METERING

The Model 115 attachments, adapters, and multiplexer channel have no meters. Instead, most I/O devices attached other than through the multiplexer channel have a usage meter, and each channel-attached device has one, either under its own covers, or in the control unit, or both.

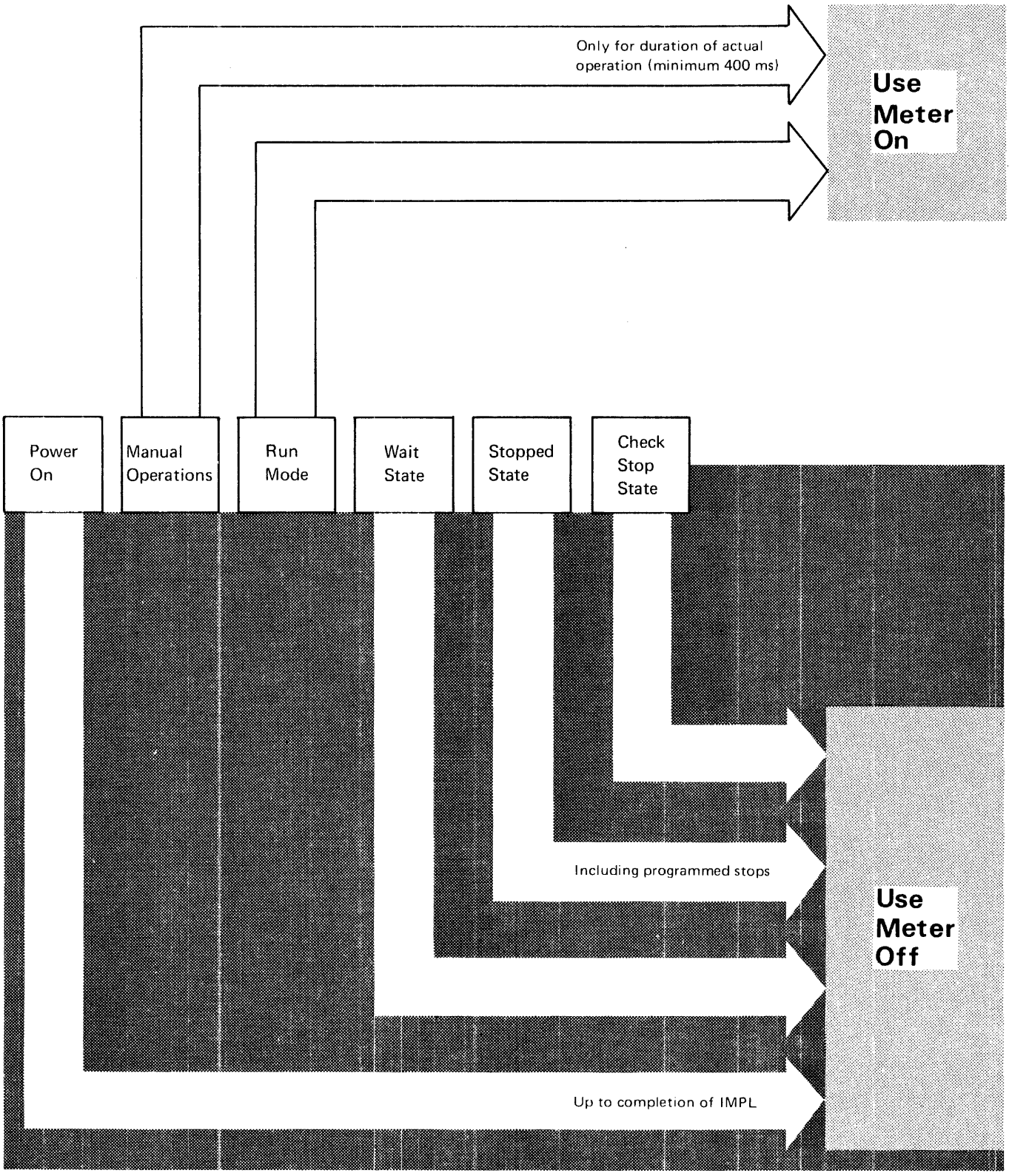
I/O metering is controlled by metering-in and metering-out lines connected to the internal bus system. The metering-in line is activated when an I/O device accepts a command, and deactivated when device end is presented for the same command. The line remains inactive for instructions, such as 'test I/O', which do not generate device end. The metering-out line is active when the system meter runs.

TELEPROCESSING METERING

For teleprocessing operations, the metering-in line is activated as soon as character transfer occurs to or from main storage.

The following types of commands do not activate metering in:

Input/Output
Enable
Disable
Set mode
Prepare
Adprep
No-operation.



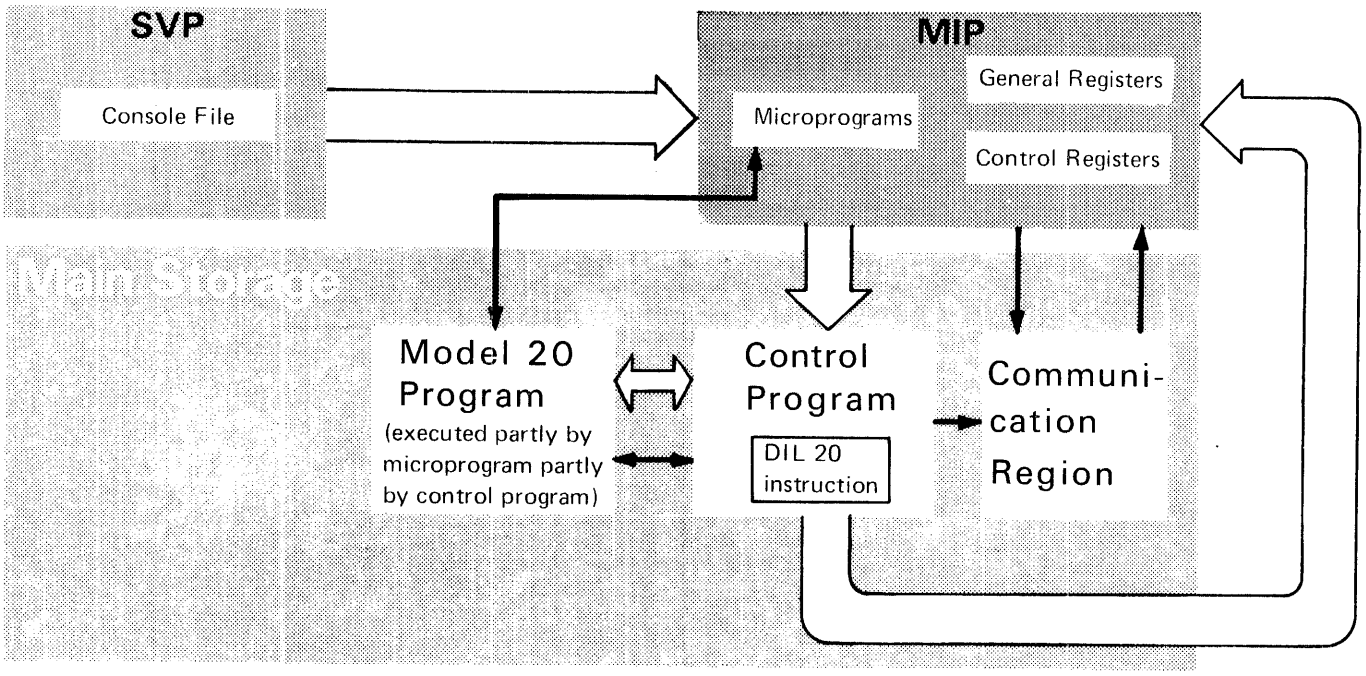
Usage Metering

Figure 51. Usage Metering [10830]

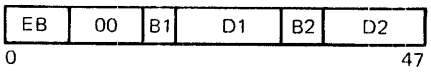
The Model 115 is designed in accordance with the principles specified in the *IBM System/370 Principles of Operation,* GA22-7000. It is therefore compatible with the other models of the System/370.

A special compatibility feature is available for emulating System/360 Model 20 operations (Figure 52).

The System/360 Model 20 Compatibility feature permits Model 20 programs to be run on the Model 115. The feature consists of a microprogram routine and the special 'do interpretive loop' instruction.



DIL 20 Format



Byte	*Contents*
0	Predefined op code EB
1	Reserved for future use
2,3	Address of first byte in communication region, 3000 (hex)
4,5	Address of displacement byte table at end of communication region, 3100 (hex).

Instruction Execution

The following Model 20 instructions are executed directly by DIL 20 microprograms without branching to a control program routine:

AR SR AH SH	Add and subtract
BCR BC	Branch on condition
CH	Compare halfword
CLI	Compare immediate
LH STH	Load, store halfword
MVI OI NI TM	Immediate operations
BASR BAS	Branch and store

All decimal instructions.

DIL 20 Functions

- Emulates Model 20 instruction fetching and checks format of instructions fetched.
- Converts address fields of Model 20 instructions and checks validity.
- Updates Model 20 instruction address and program error condition codes.
- Performs linking and branching.

Communication Region

The communication region contains:

- First two bytes of Model 20 instruction
- Model 20 current PSW
- Address relocation factor and highest Model 20 address
- Address of program error stop and interruption routines
- Model 20 pending interruptions, with priority.

Model 20 Compatibility Feature

Figure 52. Model 20 Compatibility Feature [10831]

The Model 115 has a direct disk attachment as a standard feature, and can also be equipped optionally with a number of other integrated attachments, adapters, and a multiplexer channel. These facilities are described in this chapter, together with the instructions available for performing input/output operations, and the characteristics of those input/output devices which are not controlled over a standard interface. The separate descriptions of I/O devices contain information on commands, status reports, sense information, and error recovery.

For a list of the input/output devices that can be connected to the Model 115 see the *IBM System/370 Input/Output Configurator,* GA22-7002.

Input/Output Operations

Input/output operations are concerned with the transfer of information between main storage and I/O devices. In the Model 115, this information transfer is handled through microprogrammed electronic controllers known as input/output processors. The IOPs are subprocessors of the system and are housed in the main frame.

Because the IOPs have a common design, they can take the processing of I/O instructions only to a certain stage. To provide the unique sequence of signals required by an attached device, specialized circuits termed *front ends* are added to the IOP. An IOP equipped with front ends forms an independent data processing unit capable of servicing a number of I/O devices.

Most front ends are designed for direct attachment of I/O devices such as card machines or a printer. In this case, the I/O device is serviced over a specialized interface and is thus under the control of an integrated attachment (Figure 53). The multiplexer channel is, however, an exception. Although this channel also consists of a front end serviced by an IOP, it operates over a standard interface, and is therefore a standard System/360 or System/370 channel.

The multiplexer channel in the Model 115 is a true channel, functionally similar to those used in the System/360. The integrated adapters and attachments have the same major characteristics as a channel and can be considered as pseudo-channels. To the operating system, therefore, all I/O devices appear to be channel-attached, and are programmed accordingly.

Operations on all I/O devices begin with a 'start I/O' instruction and are implemented through channel command words. The non-channel-attached devices transmit status information like those which are channel-attached, and request program interruptions for conditions such as channel end and device end.

CHANNEL ORGANIZATION

For programming purposes, the Model 115's facilities for the attachment of I/O devices are considered to consist of three channels (Figure 54). The multiplexer channel is suitable for attaching the System/360 and System/370 control units shown in *System/370 Input/Output Configurator,* GA22-7002. The integrated adapters, integrated attachments, and direct disk attachment require no external control units, but are connected directly to the I/O devices. The channel organization of the Model 115 is described in the following paragraphs.

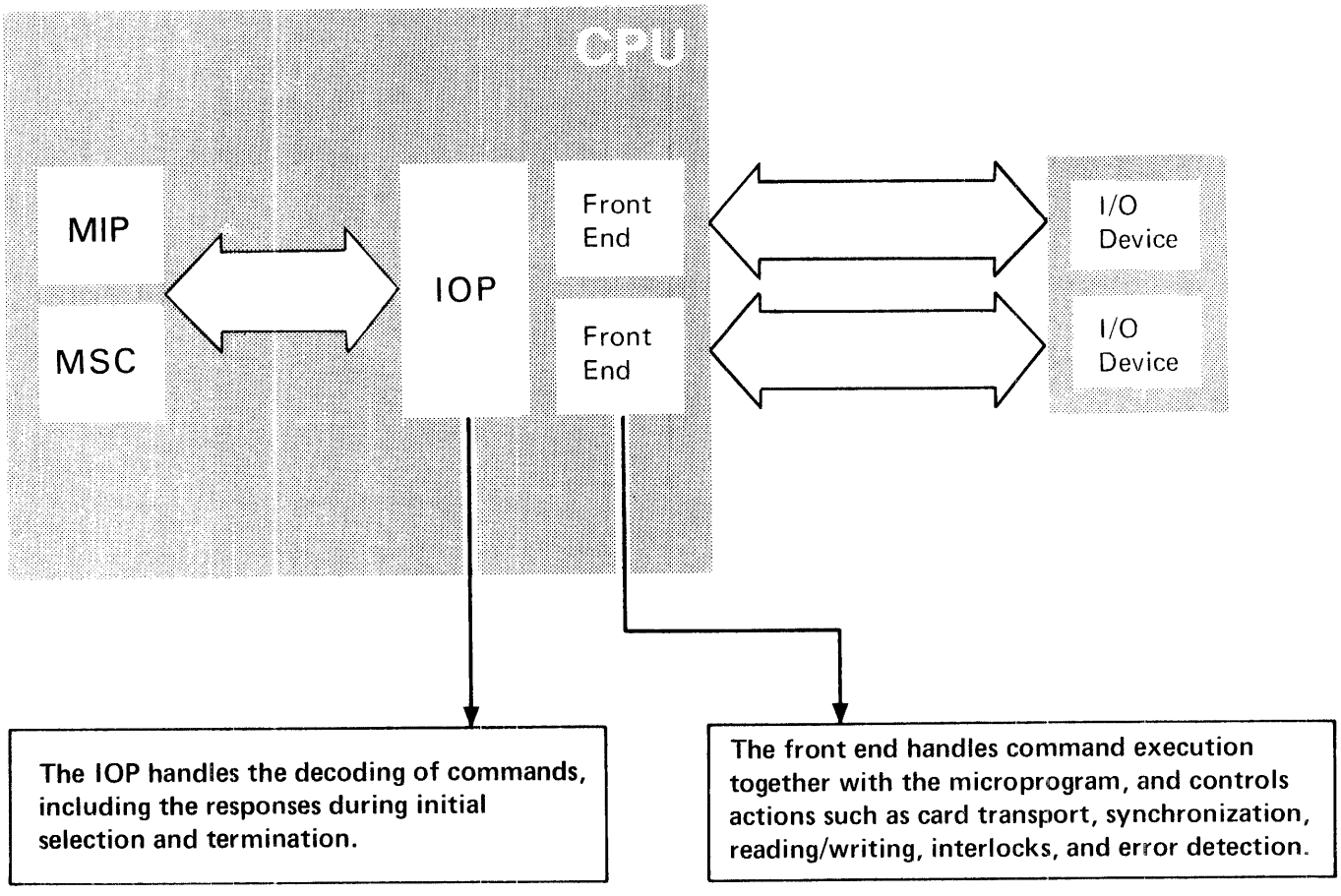
Integrated Adapters and Attachments

An integrated adapter or attachment consists of an IOP and specialized front end circuits. Integrated attachments may share an IOP, or wholly occupy an IOP, depending on the complexity of their tasks. For example, the integrated attachments for the line printer and the card I/O devices all share one IOP.

Integrated adapters, integrated attachments, and a direct disk attachment are available for the following input/output devices:

- 2560 Multi-Function Card Machine
- 5425 Multi-Function Card Unit
- 5203 Printer
- 3203 Printer
- 3410 Magnetic Tape Unit and 3411 Magnetic Tape Unit and Control
- 3340 Disk Storage

In addition, an integrated communications adapter is available.



Integrated Adapters and Attachments

Figure 53. Integrated Adapters and Attachments [10832]

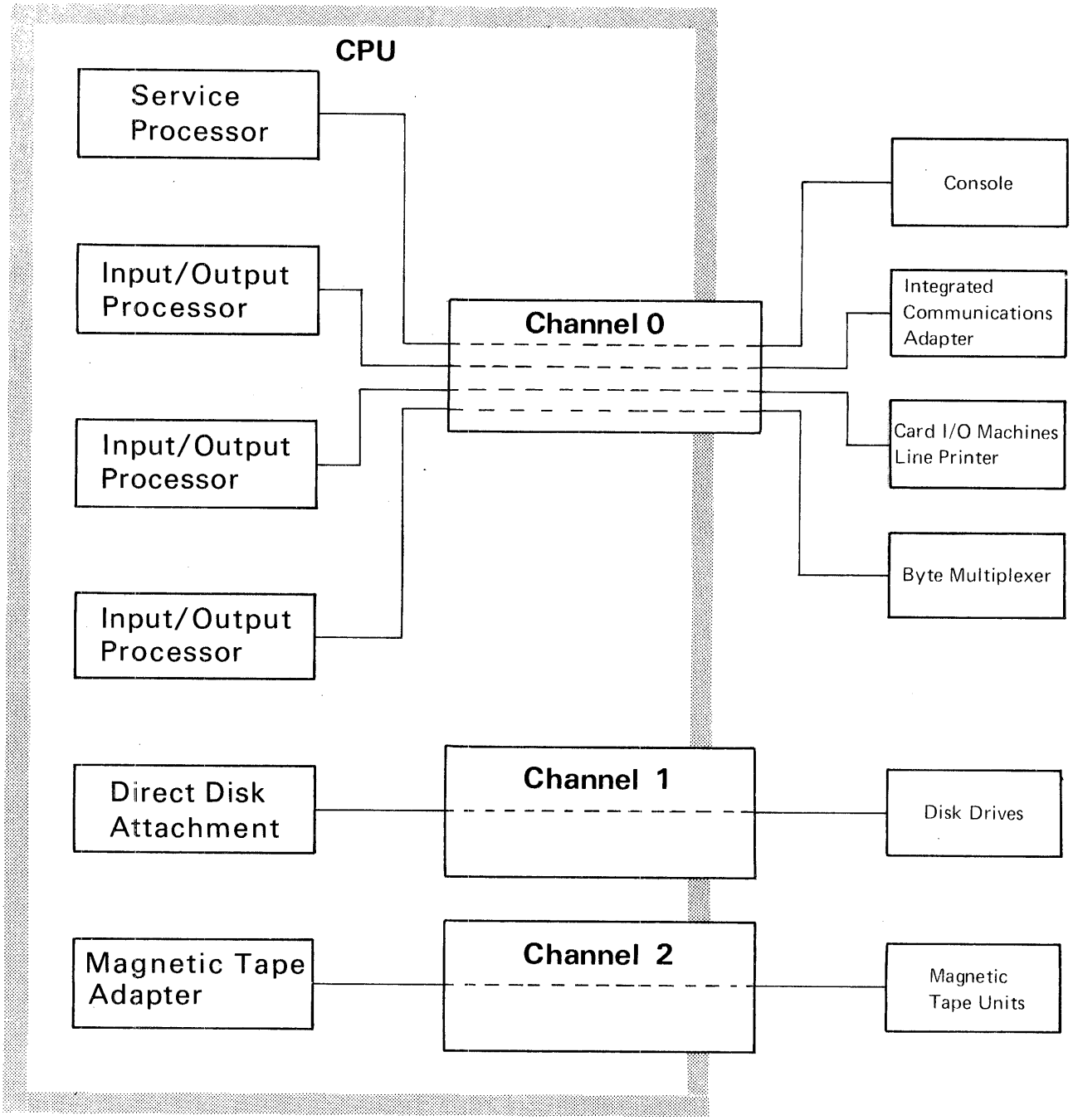


Figure 54. Channel Organization [10833]

Channel 0

Channel 0 is a pseudo-channel (Figure 55). Its overall behavior is that of a multiplexer channel. The Model 115 subprocessors operating in channel 0 do not behave like subchannels (as might be expected), but like true channels (see Figure 55).

Subprocessor	Functional Behavior
SVP serving operator console and console printer	Selector channel with single device attached
IOP serving integrated communications adapter	Multiplexer channel with a number of subchannels
IOP serving card I/O machines and line printer	Selector channel with three control units, each having one device attached
IOP serving multiplexer channel	Multiplexer channel with a number of subchannels

Figure 55. Channel 0 Definition [10834]

The I/O devices on channel 0 have unique and fixed addresses (Figure 56). Interruptions are always considered to be pending in the device, not in the control unit or subchannel.

Channel 1

Channel 1 is the direct disk attachment for magnetic disk drives. A standard interface is not available but the behavior is that of a selector channel with a shared control unit attached.

Channel 2

Channel 2 is the magnetic tape adapter for magnetic tape units. It behaves like a selector channel with a shared control unit attached.

Channels 3, 4, and 5

Channels 3, 4, and 5 are not assigned on the Model 115.

Device Selection

Device selection is performed in two major steps. The first step is the selection of the IOP responsible for the addressed device; the second step is selection of the actual I/O device.

Input/output instructions are detected by the machine instruction processor in the program instruction stream. The MIP computes and checks the channel and device addresses, and places the complete address in the I/O communication register, which is located in the main storage controller's local storage. Subsequently, the MIP activates the select line to the appropriate IOP.

The MIP has a separate select line to each of the IOPs in the system. A check ensures that multiple selection cannot take place undetected. At the time the select line is activated, a 1.5 second timeout is started. The selected IOP then fetches the contents of the I/O common register, inspects them, and activates the common response line to the MIP.

Upon detection of the response, the MIP resets the timeout, checks the channel address word for validity and places the channel command word address (designated by the CAW) and an abbreviated operation code (for 'start I/O', 'halt I/O', 'halt device' or 'test I/O' instructions) into the I/O communication register. The MIP then deactivates the select line.

The termination of the select signal causes the IOP to fetch the CCW, solicit the device response, and subsequently to store a condition code into the I/O communication register. The IOP announces the availability of the condition (and status where appropriate) to the MIP by deactivating the response line. At this moment the MIP is released for further processing, and the IOP handles data transfer.

In the event of a timeout (no response) or wrong selection (wrong IOP number in the I/O communication register) the MIP recognizes a channel control check and updates the channel status word (CSW) accordingly. Unusual conditions such as IOP busy or IOP not operational are indicated to the MIP via direct control lines which are assigned these meanings. The appropriate status updating is then also handled by the MIP.

Over similar control lines, the MIP indicates to the selected IOP the current control mode (EC or BC), and also signals the status of the system meter. The IOP thus has all the information required for processing.

Interruption requests are generated by the IOP and sent via the interruption request line to the MIP. Each IOP has its own separate interruption request line that identifies the requesting IOP. The MIP handles the interruption task by analyzing the contents of the masks and by exchanging the program status words if appropriate.

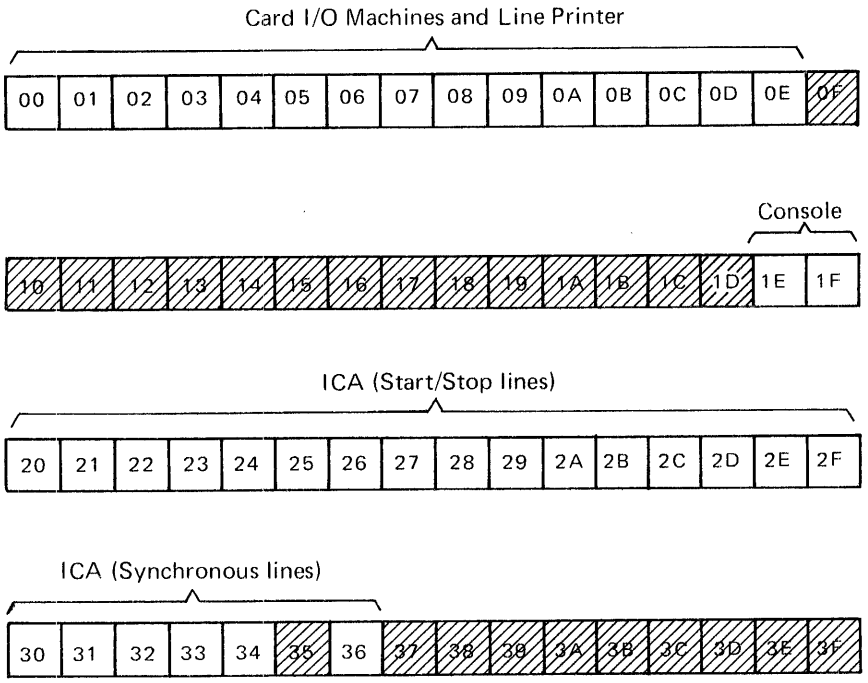
Multiplexer Channel

A byte multiplexer channel (channel address 0) with a maximum of 32 subchannels is available as an optional feature, if the Model 115 is not equipped with the integrated card I/O attachment. The byte multiplexer channel has a standard I/O interface with bus and tag line connector for attaching external control units of the shared or nonshared type. High-speed data transfer with data-in and data-out tag lines is not provided on the multiplexer channel. The control units can operate in multiplex mode or burst mode.

In function, the byte multiplexer channel conforms to the definitions given in *IBM System/370 Principles of Operation*, GA22-7000. The byte multiplexer channel is intended for the attachment of a relatively large number of

I/O Device Addresses

I/O device addresses are derived from the contents of the base register referenced by an I/O instruction, and the displacement contained in the instruction. The I/O address is calculated by the MIP which then selects the appropriate IOP or other subprocessor. The address ranges of attachable I/O devices operating in channel 0 are shown below.



Note: The above devices operate in channel 0. In all other channels, the device addresses depend on the control units or devices only: the MIP recognizes only the channd address. The device addresses range from 00 to FF (hex), and are decoded by the control units or their equivalents.

= Not used

Addressing I/O Devices Operating in Channel 0

Figure 56. Addressing I/O Devices Operating in Channel 0 [10835]

low-speed I/O devices. When the channel is working in byte multiplexer mode (its normal mode of operation), several I/O devices can execute commands simultaneously by interleaved byte transfers over the I/O interface. However, a control unit capable of forcing burst mode may do so.

The multiplexer channel performs the following functions:

Interprets I/O instructions,
Translates I/O instructions into commands and controls at the interface,
Transfers data between I/O devices and main storage,
Requests interruptions.

The functions of the byte multiplexer channel are provided by an IOP, supplemented by front end circuitry. In byte multiplexer mode, the maximum channel data rate is 19,000 bytes per second. In burst mode, the maximum channel data rate is 29,000 bytes per second. When data chaining and channel indirect data addressing are specified in the CCW, the data rates decrease to 13,000 and 19,000 bytes per second, respectively.

Characteristics

The byte multiplexer channel provides all the functions necessary to process channel programs written according to the definitions in *System/370 Principles of Operation,* GA22-7000. The channel can operate in BC mode (when PSW bit 12 is off) or EC mode (when PSW bit 12 is set).

Note: All I/O instructions can be executed, but one exception should be noted. Although the 'start I/O fast release' instruction is accepted, it is executed as a normal 'start I/O' instruction.

Of the extended interface capabilities provided by the extensions to the System/360, the multiplexer channel implements only the I/O Error Alert function. It does not implement High-Speed Transfer, Interface Bus Extension, or Command Retry. These restrictions, however, do not affect the capability of attaching and operating all I/O devices which have data rates compatible with the channel.

Subchannels

Up to 32 subchannels can be provided for the byte multiplexer channel. A subchannel, also called a unit control word (UCW), holds the information necessary for controlling the current operation in the I/O device.

A subchannel may be shared or nonshared. A shared subchannel is used for a control unit that can have several devices attached, only one of which requires the subchannel at any one time. A nonshared subchannel is used for a control unit to which only one device is attached. Of the 32 subchannels available on the Model 115 the first eight can alternatively operate as shared subchannels. Each control unit associated with a shared subchannel may have up to 16 I/O devices attached.

When a subchannel is addressed by an I/O instruction, bit 0 of the address byte (Figure 57) shows whether the subchannel is nonshared (bit 0 = 0) or shared (bit 0 = 1). Bit 0 is not, however, part of the actual address and is ignored for addressing purposes. A nonshared subchannel is addressed by the seven low-order bits of the address byte. Device addresses 40 to 7F (hex) are available, subject to the restrictions noted in Figure 57.

A shared subchannel is addressed in terms of the associated control unit. Device addresses 80 to FF (hex) are available, subject to the restrictions noted in Figure 57. Bit 0 is ignored for addressing purposes, and bits 1, 2, and 3 address the subchannel. Bits 4 through 7 are used to address an I/O device or the shared subchannel. Thus, device addresses 90 through 9F, for example, all address shared subchannel 1. Because shared subchannels 0 through 7 use the same unit control words as nonshared subchannels 0 through 7, shared subchannel addresses must be chosen which do not conflict with nonshared subchannel addresses.

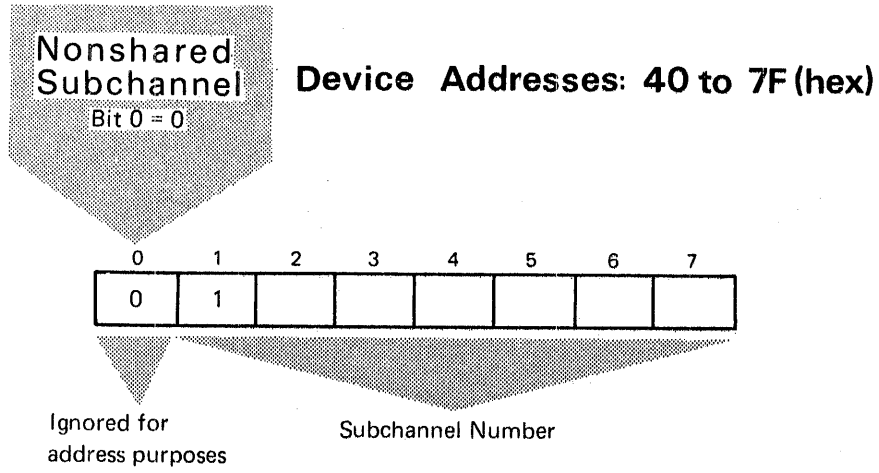
Interruption

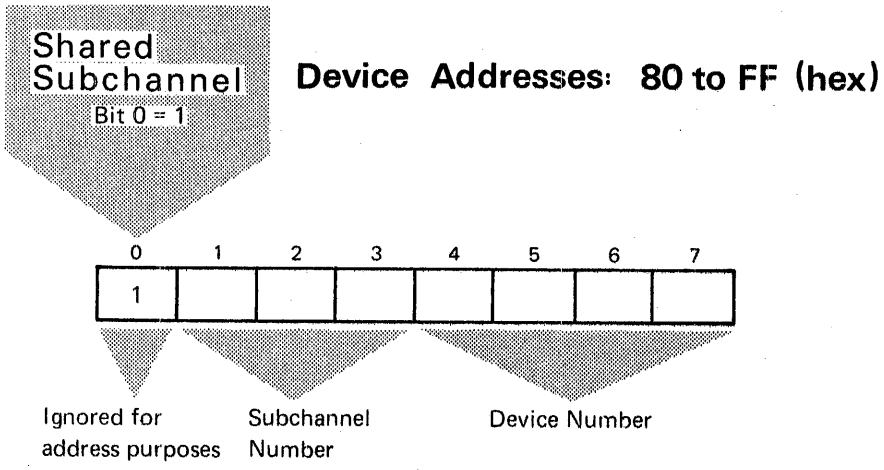
Channel end status can be signaled by up to 32 control units and stored in the corresponding subchannels. Over a single interruption line, the MIP is informed that the multiplexer channel has interruptions waiting. When the MIP signals its readiness to process an interruption for the multiplexer channel, the microprogram selects one of the waiting interruptions and signals the address of the interrupting device to the MIP. The channel stores the CSW and releases the MIP.

Error Detection

The following types of errors are detected and logged by the multiplexer channel:

1. All *programming errors.*
2. *Protection check,* which occurs when a protected address is encountered during data transfer or chaining.
3. *Channel data check,* which occurs when bad parity is detected during transfer of data to or from main storage.
4. *Channel control check,* which occurs when bad parity is detected during transfer of control information to or from main storage, or from the IOP to the channel front-end registers.
5. *Interface control check,* which can occur when bad parity is detected in an address or status byte being transferred to main storage, or when more than one tag line is activated. Interface control check also occurs when an incorrect address is received by the channel in response to 'address out', or when an address is received from an I/O unit for which no UCW is assigned.





Note: Certain restrictions apply to address assignment. In any one row of the following table, only *one* of the three address assignments can be chosen for devices which are to operate simultaneously. Taking the first row, for instance, if address 40 (hex) is assigned, addresses 60 (hex) and 80 through 8F (hex) should not be assigned.

Nonshared Subchannels (hexadecimal)		Shared Subchannels (hexadecimal)
40	60	80 to 8F
41	61	90 to 9F
42	62	A0 to AF
43	63	B0 to BF
44	64	C0 to CF
45	65	D0 to DF
46	66	E0 to EF
47	67	F0 to FF
48	68	
49	69	
4A	6A	
4B	6B	
4C	6C	
4D	6D	
4E	6E	
4F	6F	
50	70	
51	71	
52	72	
53	73	
54	74	
55	75	
56	76	
57	77	
58	78	
59	79	
5A	7A	
5B	7B	
5C	7C	
5D	7D	
5E	7E	
5F	7F	

Address Bytes for Byte-Multiplexer Subchannel

Figure 57. Address Bytes for Byte-Multiplexer Subchannel [10836]

Input/Output Control

INPUT/OUTPUT INSTRUCTIONS

The integrated adapters, integrated attachments, direct disk attachment, and multiplexer channel are controlled by the following I/O instructions:

Start I/O (fast release is *not* implemented)
Test I/O
Halt I/O
Halt device
Test channel
Store channel ID,

to which the following rules apply:

1. During execution of an I/O instruction, if an error status (such as a channel data check, a channel control check, or an interface control check) is stored, a limited channel logout is available at storage location 176.
2. For all I/O interruptions that occur in EC mode, the full three-byte address is available at storage location 184.
3. The instructions have the same function in EC and BC mode.

Start I/O

The 'start I/O' instruction is used to initiate operations in I/O devices.

Effect

The B1/D1 field specifies a channel, subchannel, control unit, and I/O device. A CCW (Figure 58) specifying the operation to be performed is sent to the device from the main storage location designated by the channel address word (CAW) residing at location 72.

The command is executed if:

1. The addressed device and subchannel are available.
2. The channel is available or has a pending interruption.
3. No errors or exceptional conditions have been detected.

Condition Code

The four values of the condition code have the following meanings assigned:

Value	*Meaning*
0	I/O operation initiated and channel proceeds with execution
1	CSW stored or updated
2	Channel or subchannel busy
3	Not operational

Note: Bit 15 may be 0 or 1 because the Model 115 has no fast release function.

Halt I/O

The 'halt I/O' instruction is used either to terminate a burst-mode operation which is occupying an interface or to terminate data transfer to or from a specific I/O device.

Effect

The 'halt I/O' instruction causes no action if the addressed subchannel has a pending interruption while the channel is either available or is in the pending interruption state.

Condition Code

The four values of the condition code have the following meanings assigned:

Value	*Meaning*
0	Interruption pending in subchannel (Halt I/O unsuccessful)
1	CSW stored
2	Burst operation terminated (interface cleared)
3	Not operational

Note: Bit 15 must be zero, otherwise the Model 115 interprets the 'halt I/O' as a 'halt device' instruction.

Halt Device

The 'halt device' instruction stops data transfer to or from an I/O device without disturbing burst-mode operations on another device.

Effect

The 'halt device' instruction stops data transfer if the addressed I/O device is operating in burst mode. 'Halt device' has no effect if it addresses a device which is not working. The effect, if any, is reflected in the condition code in conjunction with the CSW.

Condition Code

The four values of the condition code have the following meanings assigned:

Value	*Meaning*
0	Subchannel is busy with another device, or an interruption is pending. (The 'halt device' instruction was unsuccessful. The instruction can be repeated successfully after interruption clearance.)
1	CSW stored. (If the unit status field is zero, the device has stopped: if this field contains busy and the status modifier [control unit busy], the device has not yet stopped. 'Halt device' need not be repeated because the channel remembers the condition and stops the device as soon as the control unit signals control unit end [busy condition ended].)
2	Channel working. (The device has not yet stopped. 'Halt device' need not be repeated, because the channel remembers the condition and stops the device as soon as its own busy condition ends.)
3	Not operational. (Manual intervention is required, otherwise 'halt device' cannot succeed. The instruction must be repeated when the operational state has been restored.)

Note: When the device has stopped, the channel is in the interruption pending state.

Test I/O

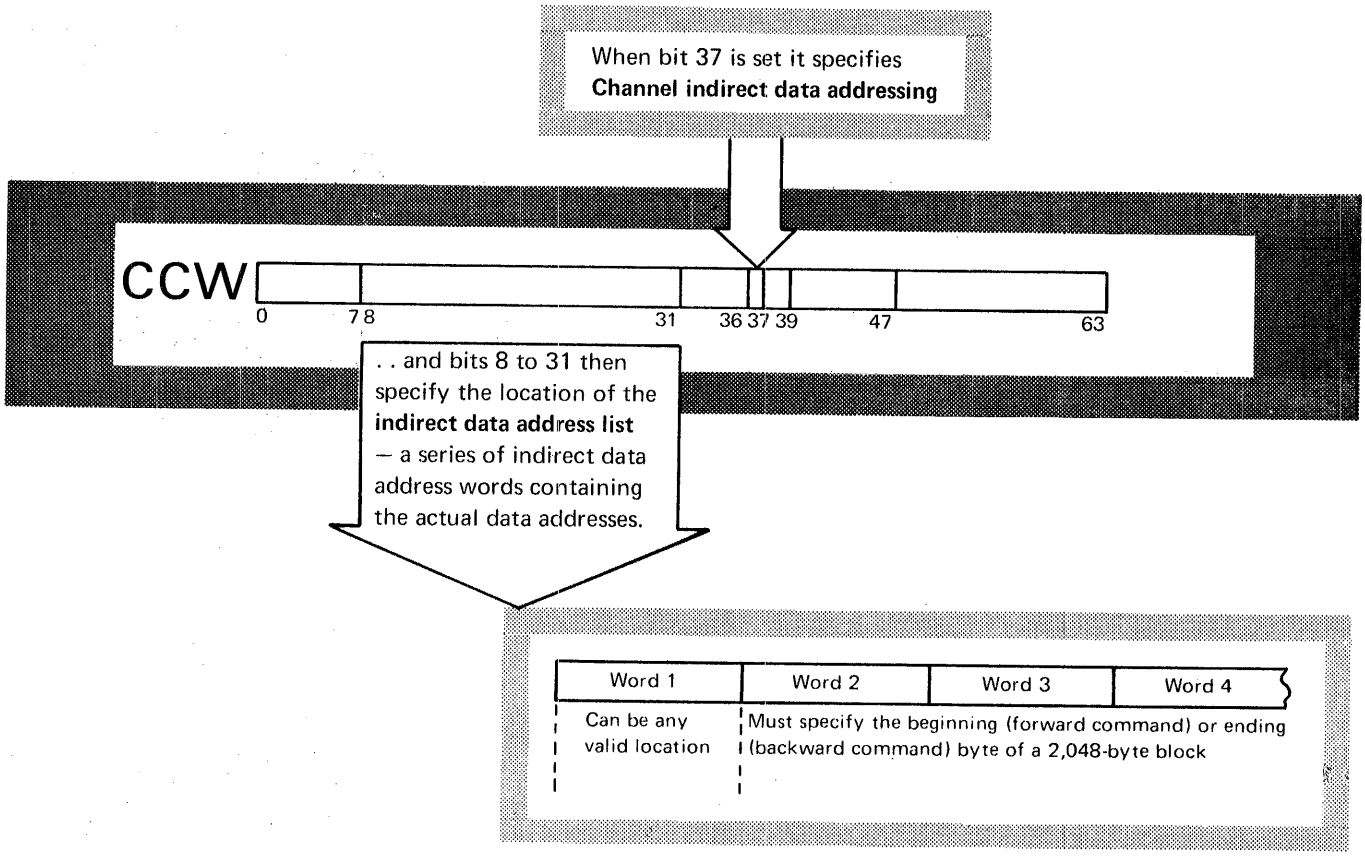
The 'test I/O' instruction tests the state of the addressed channel, subchannel, and I/O device.

Channel Command Words

The CCWs specify operations to be performed on I/O devices connected to the multiplexer channel or to an integrated adapter or attachment. All I/O devices use the applicable commands from the following:

- Write
- Read
- Read backward
- Control
- Sense
- Transfer in channel.

This also applies to devices previously not available for channel attachment such as the 5425 Multi-function Card Unit. Each command functions in the same way in BC or EC mode. All flag bits are available for I/O devices connected to the multiplexer channel or to an integrated adapter or attachment, unless otherwise stated in the command descriptions (for further information, see the descriptions of I/O devices later in this chapter). For some operations the use of certain flag bits is not recommended. In teleprocessing, for example, chaining from a 'write' to a 'read' command is necessary for obtaining an acknowledgement. In this situation, skipping or program-controlled interruptions should be avoided.



Note: When the channel has filled or read out a block, the next address word is fetched. Since the channels pre-fetch address words, CCWs must not modify the indirect data address list. If indirect data addressing and DAT are used together, PCI should not be used

Additional Information on CCWs

Figure 58. Additional Information on CCWs [10837]

Effect

The B1/D1 field identifies the channel, subchannel and I/O device to be tested. The test result is reflected in the condition code, or in the condition code and CSW together. The 'test I/O' instruction can be used to clear pending interruptions.

Condition Code

The four values of the condition code have the following meanings assigned:

Value	*Meaning*
0	Available
1	CSW stored
2	Channel or subchannel busy
3	Not operational

Test Channel

The 'test channel' instruction can test the state of the multiplexer channel, integrated adapters, integrated attachments, or the direct disk attachment.

Effect

The B1/D1 field identifies the channel to be tested. The result is reflected in the condition code.

Condition Code

The four values of the condition code have the following meanings assigned:

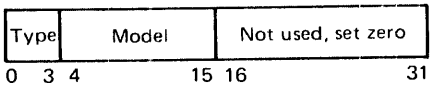
Value	*Meaning*
0	Channel available
1	Interruption pending in channel
2	Channel operating in burst mode
3	Channel not operational

Store Channel ID

The 'store channel ID' instruction checks the identity (type and model number) of the addressed channel, adapter, or attachment.

Effect

The B1/D1 field specifies the channel that is to identify itself. The identification is stored at main storage location 168 in the following format:



Type (Bits 0 to 3): Bits 0 to 3 identify the present channel characteristics and functional behavior as follows:

Value	*Meaning*
0000	Selector type
0001	Byte multiplexer
0010	Block multiplexer

Model (Bits 4 to 15): The model number identifies the channel address. (See Figure 26.)

Extended I/O Logout (Bits 16 to 31): Bits 16 to 31 specify the maximum length of an I/O extended logout. For the Model 115 this length is zero because I/O extended logouts are not performed. The error log for channel hardware is recorded on the console file. Error information concerning externally-connected control units and their I/O devices must be obtained via 'sense' commands.

Condition Code

The four values of the condition code have the following meanings assigned:

Value	*Meaning*
0	Channel ID stored correctly
1	CSW stored
2	Channel activity prevented storage of ID
3	Not operational

INPUT/OUTPUT COMMANDS

A channel, adapter, or attachment can execute six types of commands: write, read, read backward, control, sense, and transfer in channel (TIC). Each command except the TIC starts an I/O operation, as described in the following sections of this chapter and in the chapter on "Teleprocessing Characteristics". The TIC command (which has a command code of 1000) allows the chaining of commands which are not located in adjacent doubleword locations in ascending order of address.

The first CCW designated by the CAW may not specify transfer in channel. When this restriction is violated, no I/O operation is initiated, and the program-check condition is generated. The error causes the status portion of the CSW with the program-check indication to be stored during the execution of 'Start I/O'.

To address a CCW on integral boundaries for doublewords, a CCW specifying transfer in channel must contain zeros in bit positions 29-31. Furthermore, a CCW specifying a transfer in channel may not be fetched from a location designated by an immediately preceding transfer in channel. When either of these errors is detected or when an invalid address is specified in transfer in channel, the program-check condition is generated. When the TIC command designates a CCW in a location protected for fetching, the protection-check condition is generated. Detection of these errors during data chaining causes the operation at the I/O device to be terminated, whereas during command chaining they cause an interruption condition to be generated.

The contents of the second half of the CCW, bit positions 32-63, are ignored. Similarly, the contents of bit positions 0-3 of the CCW are ignored.

IBM 2560 Multi-Function Card Machine, Models A1 and A2

This section describes the commands, status reports, sense information, and error recovery procedures for the 2560 Multi-Function Card Machine (MFCM) Models A1 and A2, when under control of the integrated card I/O attachment.

Two models of the 2560 can be attached to the Model 115. The main differences between them are that the Model A1 has five stackers, and can be equipped with the optional Card Print feature; the 2560 Model A2 has four stackers and cannot be equipped with the card print feature.

2560 COMMANDS

Figure 59 shows the commands available for the 2560.

Command Code									Command
Hex	CCW Bits 0	1	2	3	4	5	6	7	
02	0	0	0	0	0	0	1	0	Read and feed primary
22	0	0	1	0	0	0	1	0	Read column binary and feed primary
82	1	0	0	0	0	0	1	0	Read and feed secondary
A2	1	0	1	0	0	0	1	0	Read column binary and feed secondary
05	0	0	0	0	0	1	0	1	Punch primary
25	0	0	1	0	0	1	0	1	Punch column binary primary
85	1	0	0	0	0	1	0	1	Punch secondary
A5	1	0	1	0	0	1	0	1	Punch column binary secondary
01	0	0	0	0	0	0	0	1	Punch and feed primary
21	0	0	1	0	0	0	0	1	Punch column binary and feed primary
81	1	0	0	0	0	0	0	1	Punch and feed secondary
A1	1	0	1	0	0	0	0	1	Punch column binary and feed secondary
45	0	1	0	0	0	1	0	1	Write card
–7	0	H	H	H	0	1	1	1	Load print head buffer
–3	0	M	M	M	0	0	1	1	Primary stacker select
–3	1	M	M	M	0	0	1	1	Secondary stacker select
–B	X	M	M	M	1	0	1	1	Punch stacker select
04	0	0	0	0	0	1	0	0	Sense
03	0	0	0	0	0	0	1	1	Control no-op

Notes:

1. The 'H' positions represent the binary coded print head buffer number.
2. The 'M' positions represent the binary coded stacker number.
3. The 'X' position in the 'punch stacker select' command may be 0 or 1; the position is ignored.

Figure 59. 2560 Commands [10838]

Read Commands

Read commands are successful only if the 2560 is in the ready state, which means that a card run-in cycle took place before the read command was issued. The run-in cycle is accomplished manually (via the 2560 START key) and ensures that the primary preread or the secondary preread stations, or both, contain cards. The run-in at the primary card path requires two cycles, one from hopper to input station, the other from input station to preread station. The run-in at the secondary path requires only one cycle, from hopper to preread station. These cycles occur simultaneously and automatically if both primary and secondary hoppers are full when the START key is pressed once.

Read and Feed Primary

The 'read and feed primary' command causes the card in the primary preread station to be moved through the read station, where the holes in the card are read column by column into an intermediate buffer. The data in this buffer is then translated to unpacked EBCDIC code and transferred to main storage while, simultaneously, a feed cycle is performed. The feed cycle moves the card in the primary input station to the primary preread station, and the bottom card (if any) in the primary hopper to the primary input station.

The read operation begins at card column 1 and continues until the count in bits 48 to 63 of the CCW is reduced to zero or until the last card column (column 80) is read, whichever occurs first. The information in card column 1 enters the main storage location specified by bits 8 to 31 of the CCW and subsequent columns are transferred to main storage in ascending order of address. Card columns which have either no holes or an invalid hole pattern are stored as EBCDIC blank characters.

Note: A hole pattern is treated as invalid when more than one hole is found in rows 1 to 7 in the same card column, except for cards punched in column binary code.

Channel end (bit 36 in the CSW) is set when the last column (in the case of command chaining, the last column of the last card) has been transferred from the intermediate buffer to main storage. The last card column is either that column which reduces the count to zero or column 80 of the card. Channel end causes an interruption condition. Device end (bit 37 in the CSW) is set when the mechanical parts of the read and feed primary operation are completed. Channel end and device end are normally set separately for a read and feed command. However, if interruptions are disabled, channel end and device end remain pending and are presented together when the interruption is cleared.

Note: Device end is always set 10 ms (–10%) prior to the clutch decision point so that the operating system has sufficient time for testing on error conditions and can thus give a new command while the clutch is still active. The setting of device end is an interruption condition.

Read Column Binary and Feed Primary

The 'read column binary and feed primary' command is similar to the 'read and feed primary' command except that the contents of the card columns are interpreted as shown in the following table.

Card Row	*Column Binary Code*	*Placed into Bits*	
12	B	2	
11	A	3	
0	8	4	First byte
1	4	5	
2	2	6	
3	1	7	
4	B	2	
5	A	3	
6	8	4	Second byte
7	4	5	
8	2	6	
9	1	7	

The information in each card column is placed into two adjacent bytes; bits 0 and 1 of each byte are automatically filled with zeros. Consequently, the count in the CCW may be twice as high as for a normal read operation, that is, any count from 1 to 160 may be specified for a 'read column binary and feed primary' command. If an odd count is specified, reading stops when the upper six rows of the card column have been read. Intermixed reading of column binary and EBCDIC columns is not possible.

Read and Feed Secondary

The 'read and feed secondary' command causes the card in the secondary preread station to be moved through the read station, where the holes in the card are read column by column. The next card is then moved from the secondary hopper into the secondary preread station.

The read operation begins at card column 1, the contents of which are transferred to the main storage location specified in bits 8 to 31 of the CCW. Reading continues with subsequent card columns which are transferred in ascending order of address until either the count in bits 48 to 63 of the CCW is reduced to zero or column 80 of the card has been transferred, whichever occurs first.

Channel end is set when the last card column has been transferred and is an interruption condition. Device end is set when the mechanical parts of the read and feed secondary operation are completed. Device end is set after channel end for a read and feed operation.

Note: Device end is always set 10 ms (−10%) prior to the clutch decision point. The setting of device end is an interruption condition.

Read Column Binary and Feed Secondary

The 'read column binary and feed secondary' command is similar to the 'read and feed secondary' command except that the contents of the card columns are interpreted as specified for the 'read column binary and feed primary' command.

Punch Commands

Punch Primary

The 'punch primary' command causes data to be transferred from main storage to the 2560 punch buffer. Data transfer begins at the main storage location specified in bits 8 to 31 of the CCW and continues in ascending order of address until either the count in bits 48 to 63 of the CCW is reduced to zero or the buffer is full (with a total of 80 characters), whichever occurs first. If the data transfer is error-free, the mechanical part of the command is then executed. If errors have occurred, the mechanical part of the punch operation is suppressed.

Note: The punch buffer need not be full, any number of characters from 1 to 80 is valid. However, the first character in the buffer will be punched into card column 1, the next into card column 2, and so on. If unpunched columns are to appear between punched columns, blank characters in EBCDIC code must be placed in the output data at the appropriate locations.

Channel end is set when the punch buffer load operation is completed. The card in the primary prepunch station is then moved into the punch station. If there is no card in the primary prepunch station, an automatic feed cycle is performed, which causes a card to be moved through the read station. This card is not read. If there is no card in the primary prepunch station and no card in the primary preread station, unit check is indicated and the no card available bit (bit 6) is set in sense byte 0). Normally the primary prepunch and primary preread stations cannot both be empty, or a hopper check would occur.

The mechanical part of the punch operation begins with card column 1 which is punched with data (translated into standard card code) from the first punch buffer location. The card is moved through the punch station column by column. Blank columns require the same amount of time as punched columns. For this reason, the information in a card should be placed as close to card column 1 as possible to obtain maximum throughput. The punch operation continues until the stored count has been reduced to zero, or column 80 has been punched, whichever occurs first. At this time, device end is set. The setting of device end is an interruption condition.

After being punched, the card stops in the punch station with the punch knives over the column following the last one punched.

Notes:

1. Although the card is stopped ready for punch continuation, a new punch command cannot punch into this same card. Instead, a new punch primary command causes a feed cycle that advances all cards (from hopper to corner station) by one station. If the new punch command is a punch secondary, an eject cycle occurs. The eject cycle causes all cards except those located before the punch station to move forward by one station. The eject cycle avoids a jam that would occur if the card in the secondary prepunch station could run into the primary card that is still in the punch station.

   The eject cycle is required whenever a 'punch only' command (which leaves the card in the punch station) is

followed by a command for the other card path. If the next command is for the same card path, the eject cycle does not occur because the respective prepunch station is empty.

2. For a punch command, device end is set 10 ms (−10%) prior to the clutch decision point, and always after the last card column has been punched.

Punch Column Binary Primary

The 'punch column binary primary' command is similar to the 'punch primary' command except that two column binary characters are punched into one card column. The punch buffer has 160 character positions because punching in column binary is a standard feature of the Model 115. It is not possible to intermix punching of column binary and EBCDIC columns.

Punch Secondary

The 'punch secondary' command is similar in function to the 'punch primary' command except that the card to be punched is taken from the secondary prepunch station.

Punch Column Binary Secondary

The 'punch column binary secondary' command is similar to the 'punch column binary primary' command except that the card to be punched is taken from the secondary prepunch station.

Punch and Feed Primary

The 'punch and feed primary' command causes data to be transferred from main storage to the 2560 punch buffer, starting at the main storage address specified in the CCW and continuing in ascending order of address until either the count is zero or the buffer is full. At this time, channel end is set in the CSW. Next, the card in the primary prepunch station is moved to the punch station and passes through it, column by column. If the primary prepunch station is empty when the command is given, an automatic feed cycle attempts to fill it.

When the last character has been punched, the feed function of the command commences. In this feed cycle, the following movements take place simultaneously:

- The card in the post-print station (or, if there is no post-print station, the card in the dummy print station) goes to the corner station and from there to the stacker.
- The card in the punch station goes to the preprint station.
- The card in the primary preread station goes through the read station (without being read) to the primary prepunch station.
- The card in the primary input station goes to the primary preread station.
- The bottom card in the primary hopper goes to the primary input station.

After these simultaneous card movements, device end is set for this command.

Punch Column Binary and Feed Primary

The 'punch column binary and feed primary' command causes the same actions as the 'punch and feed primary' command except that column binary characters are punched.

Punch and Feed Secondary

The data transfer and mechanical actions initiated by the 'punch and feed secondary' command are similar to those initiated by the 'punch and feed primary' command, except that all card movements take place in the secondary card path.

Punch Column Binary and Feed Secondary

The 'punch column binary and feed secondary' command is similar to the 'punch column binary and feed primary' command except that it deals with cards in the secondary card path.

Load Commands

Load commands may only be given to a 2560 Model A1 that has the optional card print feature installed.

Load Print Head Buffer

The 'load print head buffer' command provides the means to load either any individual print head buffer or all available print head buffers. Depending on the number of heads installed, either two, four or six print head buffers are available. Command code bits 1, 2, 3 (denoted as H, H, H in Figure 59) have the values 4, 2, 1 assigned and are thus capable of representing any number from 0 to 7. The number thus specified determines the buffer to be loaded and the loading method as follows:

Number 0 (all three bits off) is invalid and causes the 'load print head buffer' command to be rejected.

Any number from 1 to 6 causes the corresponding print head buffer to be loaded, but only this buffer. The maximum byte count for such an operation is 64. If the byte count is less than 64, the remaining buffer positions are not changed and will therefore retain previous data (if any). If the specified buffer is not installed, the command is rejected.

Number 7 causes all six buffers to be loaded sequentially, beginnning with buffer 1 and ending with buffer 6 (unless the length count is insufficient). The maximum byte count for such an operation is 384. If the byte count is less than 384, the remaining buffers are filled with blanks. If less than six buffers are installed, the command ends normally when the last available buffer has been loaded (or filled with blanks). The 'load print head buffer' command can thus be used to delete previous contents or to find out how many buffers are installed.

The 'load print head buffer' command causes data to be transferred from main storage to the print head buffer(s). The data transfer begins at the main storage location specified in bits 8 to 31 of the CCW and continues in ascending order of address until either the specified buffer or all buffers have been filled or the count in bits 48 to 63 of the CCW is reduced to zero, whichever occurs first. At this time channel end and device end are both set in the CSW. Data thus stored in the print head buffers remains valid until overwritten by another load operation or until power goes off. After power-on, all buffers are filled with blanks (hex 40).

Note: If the 'load print head buffer' command is given at a time when there is no card at the preprint station, unit check (bit 38 in the CSW) is set and a 'sense' command will then show the no card available bit (bit 6 of sense byte 0) as the cause. A subsequent read and feed, punch, or punch and feed command will then provide a card at the preprint station.

Write Commands

Write commands may only be issued to a 2560 Model A1 that has the optional card print feature installed.

Write Card

The 'write card' command causes a data byte that contains the selected print head to be transferred from main storage, after which the print operation starts. The selected print head prints the contents of the assigned print buffer under control of the length count for the 'write card' command.

The print head selection byte is fetched from the main storage location addressed by bits 8 to 31 of the CCW. The bits in this byte designate the individual print heads of the machine as follows:

Bit	*Print Head*
0	1
1	2
2	3
3	4
4	5
5	6
6	(Ignored)
7	(Ignored)

A print head is selected when its corresponding select bit is set. Any combination of print heads is valid except no selection, when bits 0 to 5 are all zeros. If no print head is selected, the 'write card' command is rejected.

If a print head is selected but its assigned print buffer has not been loaded, the 'write card' command is executed but only blanks are "printed". If a print head is selected which is not installed in the machine, the card is stepped through the print station without printing and no error indication is given. If, however, a 'write card' command is issued to a 2560 without the card print feature, the command is rejected.

After the print head select byte is transferred, the printer control is started and then channel end and device end are both set.

Note: The device end indication for the 'write card' command is deliberately presented at the beginning of the mechanical print operation so that a punch command can be accepted following the 'write card' command. This allows punch operations to fully overlap card print operations.

After channel end and device end for a 'write card' command have been presented, the 2560 appears busy for all other commands except punch commands until the mechanical print operation is completed. This is not, however, indicated by the busy bit (bit 35) in the CSW. Instead, any subsequent 'write card' or 'load print head buffer' command is rejected with unit check set in the CSW and the no card available bit set in sense byte 0. This means that a 'write card' command must be followed by a read and feed or a punch command before another 'write card' command can be given.

If there is no card in the preprint station when a 'write card' command is given, an automatic eject cycle is performed, provided a card is available in the punch station. If there is no card in either the preprint or the punch station (both stations empty), the 'write card' command ends with unit check set and the no card available bit set in sense byte 0.

The mechanical part of the print operation consists of moving the card at the preprint station into the print station. The entire card is then moved through the print station, column by column, and the print heads print characters onto its surface.

Stacker Select Commands

Note: If a stacker select command selecting stacker 5 is given to a 2560 Model A2, the command will be executed as a stacker select command to stacker 4.

Primary Stacker Select

The 'primary stacker select' command provides a means of directing a card in the primary path to a stacker other than the normal destination. The normal destination for primary cards is stacker 1, which is automatically selected in the absence of a stacker select command.

The 'primary stacker select' command is of the control immediate type; only the command code is transferred to the card I/O front end and channel end is indicated in the initial status. Device end is set when the select information has been set internally.

The command code carries the stacker select information in bits 1, 2 and 3 of the command byte (shown as M, M, M in Figure 65). Bits 1, 2, and 3 have the following binary values assigned:

Bit	*Binary Value*
1	4
2	2
3	1

Any value from 1 to 5 (decimal) is valid. Any value above 5 causes the command to be rejected. If the 'primary stacker select' command has the value zero, it is treated in the same way as a 'control no-op' command and causes only status presentation.

The 'primary stacker select' command is always assigned to the card located in the primary prepunch station at the time the command is given. Since it cannot be assumed that a card is actually located in the primary prepunch station at this time, it is recommended that the 'primary stacker select' command should be given either *after* a read and feed command for that card or, if reading is not intended, *before* the next punch or punch and feed command is given for the primary card path.

These rules for command placement ensure that stacker selection can be assigned either to a card that is already in the primary prepunch station (as is the case after a read and feed operation) or to a card that will arrive at the primary prepunch station (as is the case with a punch or punch and feed operation).

Note: A 'primary stacker select' command that is issued either before a read and feed, or after a punch or punch and feed command for a card will not change the normal selection (stacker 1) for that card. A 'primary stacker select' command also has no effect if given immediately after card run-in.

Secondary Stacker Select

The 'secondary stacker select' command provides a means of directing a card in the secondary card path to a stacker other than the normal destination. The normal destination for secondary cards is stacker 5, which is automatically selected in the absence of a stacker select command.

The 'secondary stacker select' command is of the immediate type; only the command code is transferred to the card I/O front end after which channel end is indicated in the initial status. Device end is set when the select information has been set internally.

The stacker select information is contained in bits 1, 2, and 3 of the command byte. Bits 1, 2, and 3 have the following binary values assigned:

Bit	*Binary Value*
1	4
2	2
3	1

Any value from 1 to 5 (decimal) is valid. Values above 5 cause the command to be rejected.

The 'secondary stacker select' command is always assigned to the card located in the secondary prepunch station at the time the command is given. Since it cannot be expected that a card is actually in the secondary prepunch station when the command is given, it is recommended that the 'secondary stacker select' command should be given either *after* a read and feed command for that card or, if reading is not intended, *before* the next punch, or punch and feed command is given for the secondary path.

These rules ensure that a stacker can be assigned either to the card already in the secondary prepunch station (as a consequence of a read and feed operation, for example), or to a card that will arrive there (as a consequence of a punch or punch and feed operation, for example).

Note: A 'secondary stacker select' command that is given either before a read and feed or after a punch or punch and feed command for a card cannot change the normal destination (stacker 5) for the card. A secondary stacker select command also has no effect if given immediately after card run-in.

Punch Stacker Select

The 'punch stacker select' command provides a means of changing the destination of *any* card whether the card is routing normally or is in a path determined by a previously-given primary or secondary stacker select command.

The 'punch stacker select' command is always assigned to the card that is either in the punch station or in the preprint station. This command can be given at any time after a read or punch command because the selection is stored and assigned to the next card that enters the print station (after the 'punch stacker select' command is given). Normally, however, the command is given in order to change a previous selection because, for example, of a punch error.

Note: The 'punch stacker select' command must be given prior to a write command. The 'punch stacker select' command should, likewise, be issued prior to the *next* read and feed, or punch, or punch and feed of any type if the destination of a card in the punch station is to be changed.

Stacker selection by the 'punch stacker select' command cannot be altered. The selection information is contained in bits 1, 2, and 3 of the command byte, as for primary and secondary stacker select commands. The command is of the immediate type, and only the command byte is transferred to the card I/O front end. Channel end is indicated in the initial status. Device end is set when the select information has been set internally.

Other Commands

Control No-Op

The 'control no-op' command causes no action at the 2560. When this command is given, channel end and device end are indicated in the initial status together with any other status indications that may exist at that time.

Sense Command

The 'sense' command retrieves the contents of the seven available sense bytes for the 2560 from the integrated card I/O attachment and transfers them to main storage. A 'sense' command should be issued whenever a 2560 operation ends with unit check set in the CSW. The error indications are placed into main storage in ascending order of the data address (CCW bits 8 to 31) up to a maximum of seven bytes, or until the count is reduced to zero, whichever occurs first. The 'sense' command does not reset the error indicators; these are reset by any next command other than 'sense' or 'control no-op', or by any instructions other than 'test I/O', 'halt I/O', or 'halt device'. For a detailed description of the sense bytes and their contents, see "2560 Sense Information" in this section.

Cycle Definitions

The foregoing command descriptions mention two types of cycles: *feed cycles* and *eject cycles.* For the benefit of programmers, these cycles are defined in the following paragraphs.

Feed Cycle

A feed cycle is either part of the command (as in read and feed, punch and feed commands) or is unsolicited. Unsolicited feed cycles occur automatically whenever a gap has developed in the card path. The purpose of an unsolicited feed cycle is to fill an empty card station so that the current command can be executed. Unsolicited feed cycles occur when a punch command of any type finds no card in the prepunch station.

Since a feed cycle always involves the entire card path, all cards from hopper to corner station advance by one station. Unsolicited feed cycles never involve reading or punching. Whether such a feed cycle affects the primary or secondary path depends on the command. Punch commands state the path explicitly (punch *primary,* punch *secondary*) and the stated path is always used by the unsolicited feed cycle.

Example: A punch command finds no card in the associated prepunch station because the previous command may have been a punch "only" command. To allow punching despite the absence of a card, an unsolicited feed cycle occurs to fill the vacated prepunch station. No reading occurs although a card moves through the read station.

Eject Cycle

The eject cycle is an unsolicited cycle that advances all cards in and behind the punch station by one station. Unlike the feed cycle, the eject cycle does not bring a new card from the hopper. The eject cycle occurs automatically for one of two purposes:

1. To clear the punch station when a jam would otherwise occur.
2. To fill the preprint station.

Examples:

1. After a punch only command for the primary path is executed, the card is still in the punch station. If the next command is some type of command for the secondary path, the card in the secondary prepunch station would collide with the card in the punch station. Thus, whenever a punch only command is followed by a command for the other card path, an eject cycle occurs automatically to clear the punch station. The eject cycle does not occur if a punch only command is followed by a command for the same card path, because the prepunch station is then empty.
2. If a write card command finds no card in the preprint station but a card is in the punch station (from a preceding punch only command), an automatic eject cycle occurs. The eject cycle does not occur if the punch station is empty. See also the description of the 'write card' command).

2560 STATUS INFORMATION

The following paragraphs describe the meanings of the status indications given in response to 2560 commands.

Unit Status

The unit status is indicated in bits 32 to 39 of the CSW. The unit status is directly related to a command that is either issued to or has been completed or terminated by the 2560. The bits are assigned the following meanings:

Bit	*Designation*
32	Attention (not used)
33	Status modifier (not used)
34	Control unit end (not used)
35	Busy
36	Channel end
37	Device end
38	Unit check
39	Unit exception

Attention (Bit 32)

The attention bit is not used.

Status Modifier (Bit 33)

The status modifier bit is not used.

Control Unit End (Bit 34)

The control unit end bit is not used.

Busy (Bit 35)

The busy bit, when set, indicates that the 2560 is busy executing a previously-initiated command. The busy bit and

the device end bit are both set when a 'start I/O' instruction is issued to a 2560 which has an initial device end interruption pending.

Channel End (Bit 36)

The channel end bit, when set, indicates that the data transfer part of a 2560 command, or the transfer of control information, has been completed. This means that received data is available in the input area or that the output area can be loaded with new data.

Device End (Bit 37)

The device end bit, when set, indicates that the 2560 has completed the mechanical part of an operation and is free to accept and execute another command. In this sense, the setting of device end marks the exact moment at which any type of busy status ends for a previously-initiated operation. For all commands that involve card movement or other clutch-dependent operations, device end is set 10 ms (−10%) prior to the next clutch decision point. If a new command is accepted prior to the clutch decision point, maximum throughput can be obtained.

Note: For a 'write card' command, device end is set so early that a punch command can be executed overlapped with card printing. Another 'write card' command will, however, set unit check with the no card available bit set in sense byte 0. Device end for the previous 'write card' command has already been given.

Device end does not itself indicate which operation has been completed at the 2560. However, if there is a command address stored in the CSW it will point to the next command to be executed. Device end is set once for each command, except during command chaining.

Device end is set alone when the 2560 is manually put into the ready state, for example – when the START key is pressed and the card run-in cycle is completed.

Unit Check (Bit 38)

The unit check bit is set for various errors or other unusual conditions that may have occurred in the 2560 or its controlling front end logic. Since the setting of unit check does not indicate which condition has occurred, a 'sense' command can be issued in order to retrieve exact information. For details of the conditions that can cause unit check to be set, see "2560 Sense Information" in this section.

Unit Exception (Bit 39)

The unit exception bit is set only for a read and feed command that has read the last card without a feed check or machine check occurring. Unit exception is set with device end for commands of this type. The card path is still in the ready state when unit exception is set. Read and feed commands as well as stacker select commands can be given to route the last card to an appropriate stacker. Read and feed commands given in these circumstances are accepted, but no data transfer occurs (the residual count will be identical with the length count in the command). For this reason, read commands given after unit exception has been set are known as *dummy* read commands. Unit exception therefore functions as the last card indicator.

Channel Status

The channel status is not specific for the 2560 but is given in conjunction with 2560 commands if these cause unusual conditions or were specified improperly. The channel status is indicated in bits 40 to 47 of the CSW, as follows:

Bit	*Designation*
40	Program-controlled interruption
41	Incorrect length
42	Program check
43	Protection check
44	Channel data check
45	Channel control check
46	Interface control check (not used)
47	Chaining check (not used)

Program-Controlled Interruption (Bit 40)

The program-controlled interruption (PCI) bit, when set, indicates that an interruption was requested because the CCW to which the status applies has the PCI flag bit set. The execution of the 2560 command is not affected by detection of the PCI flag, however. The PCI bit also indicates that the interruption may be expected to take place as soon as possible. The actual time at which the PCI occurs cannot be predicted (masking or other activities can cause delays).

Incorrect Length (Bit 41)

The incorrect length bit is set whenever the number of bytes in the main storage input or output area assigned to a 2560 operation is not equal to the number of bytes offered or requested by the 2560. For example, the maximum number of print positions is 64 and the maximum number of card columns is 80 and these maximum numbers are the checking criteria for incorrect length. Thus if the length count for a 'write card' command is less than 64, incorrect length is indicated and the residual count is zero. If the length count is greater than 64, incorrect length is indicated and the residual count shows the number of bytes not transferred. The incorrect length indication is suppressed when the current CCW has the SLI flag bit set and the CD flag bit off, or the current CCW is an immediate command or is rejected.

Program Check (Bit 42)

The program check bit, when set, alerts the program to various error conditions (described in the following text) that may be caused by incorrect specifications or an invalid command sequence.

1. *Invalid CCW Address Specification.* The CAW or the transfer-in-channel command does not designate the CCW on an integral doubleword boundary (the address is not a multiple of eight).
2. *Invalid CCW Address.* The card I/O attachment attempts to fetch a CCW from a location outside main storage.
3. *Invalid Indirect Data Address List (IDAL).* The origin address of the IDAL is not on a word boundary. This case applies only when CCW bit 37 is set.
4. *Invalid Indirect Data Address Word (IDAW).* Bits 0 to 7 of the IDAW are not zero, or the second and subsequent address words do not specify the first or last byte of a 2,048-byte block. This case applies only when CCW bit 37 is set.
5. *Invalid Command Code.* The command code in the first CCW addressed by the CAW or the first CCW of a chain contains four low-order zeros.
6. *Invalid Count.* A CCW (other than for a TIC command) contains the value zero in bits 48 to 63 (the count field).
7. *Invalid Data Address.* The card I/O attachment attempts to fetch data from a location outside addressable main storage. This may occur because either the CCW contains an invalid data address or the main storage controller modifier has updated the address beyond the upper limit.
8. *Invalid CAW Format.* The channel address word does not contain zeros in bit positions 4 to 7.
9. *Invalid CCW Format.* The CCW (other than for a TIC command) does not contain zeros in bit positions 37 to 39.
10. *Invalid Sequence.* The first CCW designated by the CAW is a TIC command, or two TIC commands are issued in succession.

Protection Check (Bit 43)

The protection check bit is set when the CAW key does not match the key of the main storage location addressed by a CCW. Protection check is also set when the addressed main storage location is protected against fetching. 2560 commands for which protection check is set are either not started or terminated.

Channel Data Check (Bit 44)

The channel data check bit is set when a parity error is detected in the data or sense information transferred between main storage and channel. Command codes, CCW or data addresses, or status reports do not set channel data check. The setting of channel data check does not terminate the operation, but chaining is suppressed. The card I/O front end forces correct parity on all data it sends or receives.

Note: If channel data check is set, a limited channel logout may be available at storage location 176.

Channel Control Check (Bit 45)

The channel control check bit is set for parity errors in the CCW address, the data address, or the CCW itself. Errors which set channel control check are severe, causing the current operation either to be not started or to be terminated immediately. Such an error usually involves the IOP or the MSC or both. The CSW in which the channel control check bit is set cannot be considered reliable.

Note: If channel control check is set, a limited channel logout may be available at storage location 176.

Interface Control Check (Bit 46)

The interface control check bit is set when a status report has invalid parity or when the 2560 is unable to respond to selection before the timeout in the MIP elapses.

Note: If interface control check is set, a limited channel logout may be available at storage location 176.

Chaining Check (Bit 47)

The chaining check bit is not used for 2560 operations.

2560 SENSE INFORMATION

The following paragraphs describe the contents of the sense bytes available for the 2560. The 2560 provides up to seven bytes of sense information, which may be transferred to main storage by use of the 'sense' command. The fact that a 'sense' command is required is indicated by the setting of unit check in the CSW.

Sense Byte 0

The bits in sense byte 0 have the following meanings assigned:

Bit	*Designation*
0	Command reject
1	Intervention required
2	Bus-out check (not used)
3	Equipment check
4	Data check
5	Feed check/machine check
6	No card available
7	(Not used)

Command Reject (Bit 0)

The command reject bit is set when either an unassigned command, or a command that requires a feature that is not installed, is given. Command reject is also set when a prerequisite condition is not met. The following conditions cause command rejection:

1. A stacker select command with an invalid stacker number (greater than 5) is given.
2. A 'write card' command is given specifying an all zeros head-selection (no selection).
3. A 'load print head buffer' command is given which specifies buffer number zero or a non-existent buffer.
4. A 'load print head buffer' command is given to a 2560 that has no card print feature installed.
5. A 'write card' command is given to a 2560 that has no card print feature installed.

Intervention Required (Bit 1)

The intervention required bit, when set, indicates that operator intervention at the 2560 is required because of one of the following conditions, any of which will cause the 2560 to lose the ready state.

1. The selected feed path (primary or secondary) is not ready or the 2560's STOP key has been pressed.
2. One of the machine covers is open (cover interlock).
3. A card is jammed in either hopper.
4. The hand wheel is engaged or the bell crank is inserted.
5. The print interlock arm is not locked, due to improper head alignment.
6. A hopper is empty.
7. A stacker is full.
8. The chip box is full or has been removed from the 2560.
9. A feed check or punch pusher check has occurred.
10. A machine check has occurred.

Bus-Out Check (Bit 2)

The bus-out check bit is not used.

Equipment Check (Bit 3)

The equipment check bit is set for "soft" errors that occurred during the execution of a command. In general, the equipment check bit is set when a feed check or machine check occurs during data transfer.

For read commands, equipment check is set when the read comparison performed in the 2560 produces an unequal result. This means that a card hole could not be read safely or a fiber optic check or read end check has occurred.

For punch commands, equipment check is set when the punch echo data shows missing or multiple punches.

In either case, the operation continues to its normal end after equipment check has been detected. Detailed information on the first failing card column is available in sense byte 6 (see "Sense Byte 6" in this section).

Equipment check is a program-resettable error. Reset occurs when the next command (of any type except a 'sense' command) is given to the 2560.

Note: If a punch circuit breaker fails during a punch command, the punch operation is not continued because punching would be unreliable. In such cases, no failing column is indicated in sense byte 6, but the 2560's PUNCH CHECK light is on.

Data Check (Bit 4)

The data check bit, when set, indicates that an invalid card code was detected in a card column during a read operation or that invalid parity was detected during loading of the punch or print buffer. The consequences of a data check are different for read and for write operations, as follows:

Data check during read: the error column is transferred to main storage as a blank character and the operation continues to normal completion (all specified columns are read).

Data check during punch buffer or print buffer loading: the load operation continues to completion and unit check is set at the same time as channel end. The mechanical portion of the punch or print operation is, however, not started.

Data check is also set if a feed check or a machine check occurs while the machine is busy executing a command, because the data transferred is not reliable.

Feed Check/Machine Check (Bit 5)

The feed check/machine check bit is used to interpret data check and/or intervention required indications. A card is wrongly positioned due to a mechanical malfunction, the 2560 went through an extra clutch cycle, or the read emitter drum was not written or was not erased. The error is in any case considered severe, so that the operation in progress is stopped. Recovery requires a non-process run-out and subsequent restart of the operation. Details about the location of the individual cards in the machine are available in sense byte 2, and details about jams or misfeeds are available in sense byte 1.

No Card Available (Bit 6)

The no card available bit is set if no card was available at the preprint station or in the punch station at the time a 'write card' or a 'load print head buffer' command was given. The no card available bit is also set if a punch command is given when both the prepunch and preread stations are empty.

Bit 7

Bit 7 is not used.

Sense Byte 1

Sense byte 1 contains detailed information about obstructions (jams, misfeeds, and so on) that caused a feed check. The individual bits are set to show where the card path was obstructed and have the following assignments:

Bit	Designation
0	Cover interlock
1	Jam bar check
2	Corner station check
3	Cell 8 to 9 feed check
4	Print station feed check
5	Punch station feed check
6	Read station feed check
7	Input station feed check

Note: All checks indicated by sense byte 1 may be reset by pressing the 2560's NPRO (non-process runout) key. The checks cause the 2560 to lose its ready state; they cannot, therefore, be reset by a new command.

Cover Interlock (Bit 0)

The cover interlock check bit, when set, indicates an open machine cover. The cover-open condition can be indicated at channel end or device end time.

Jam Bar Check (Bit 1)

The jam bar check bit, when set, indicates that a card jammed above the stackers or at the pocket entry. This check can be set at channel end or device end time.

Corner Station Check (Bit 2)

The corner station check bit, when set, indicates that a card was not ejected from the corner. This check can be set at channel end or device end time, or be presented for the next command.

Cell 8 to 9 Feed Check (Bit 3)

The cell 8 to 9 feed check bit, when set, indicates that a card was obstructed or did not leave the area after the print station so that it did not arrive at the corner station. This check is set at channel end time.

Print Station Feed Check (Bit 4)

The print station feed check bit, when set, indicates that a card was not fed from the preprint station through the print station. This check is set at device end time.

Punch Station Feed Check (Bit 5)

The punch station feed check bit, when set, indicates that a card was not ejected out of the punch station into the preprint station. This check is set at device end time.

Read Station Feed Check (Bit 6)

The read station feed check bit, when set, indicates that a card was not fed through the read station, was already in the read station at the start of the cycle, or is still in the read station at the end of the cycle. This check is set at device end time.

Input Station Feed Check (Bit 7)

The input station feed check bit, when set, indicates that a card did not leave the input station. This check is set at device end time.

Sense Byte 2

Sense byte 2 contains information on the location of individual cards in the 2560 at the beginning of the cycle in which a feed check or machine check was detected. The bits in sense byte 1 have the following meanings assigned:

Bit	Designation
0	Secondary select
1	Card in punch station
2	Preprint SC 7 exposed
3	Prepunch SC 5 exposed
4	Prepunch SC 4 exposed
5	Preread SC 3 exposed
6	Preread SC 2 exposed
7	Input station SC 1 exposed

Secondary Select (Bit 0)

The secondary select bit, when set, means that the secondary card path was selected during execution of the previous command. If the secondary select bit is at zero, the primary path was selected. If neither path was selected, the state of the secondary select bit is unpredictable.

Card in Punch Station (Bit 1)

The card in punch station bit, when set, means that a card is in the punch station.

Preprint SC 7 Exposed (Bit 2)

The preprint SC 7 exposed bit, when set, means that there is no card in the preprint position. When the solar cell (SC) in this position is covered by a card, the bit is at zero.

Bits 3 to 7

Bits 3 to 7 are operated by solar cells in the same way as bit 2. The odd-numbered solar cells (1, 3, 5) sense cards in the primary card path; the even-numbered solar cells sense cards in the secondary path.

Sense Bytes 3, 4, and 5

Sense bytes 3, 4, and 5 contain the stacker select information for all cards throughout the 2560. The contents of these three sense bytes represent a replica of the stacker select registers so that the origin and destination of the last stacked card, the card to be stacked, and so on can be determined for error recovery or restart procedures.

The information in sense bytes 3, 4, and 5 should be examined whenever feed checks or machine checks occur or when other errors require new job set-up. The information enables cards in the stacker to be identified after a runout and to be placed into the correct original hopper for a restart.

Sense Byte 3

Sense byte 3 contains the stacker selections assigned to cards at the primary and secondary prepunch stations, as shown in the following table.

Bit	*Meaning*	*Card Location*
0	primary card 0	Primary prepunch station
1	binary value 4	
2	binary value 2	
3	binary value 1	
4	secondary card 1	Secondary prepunch station
5	binary value 4	
6	binary value 2	
7	binary value 1	

Bit 0 is permanently at zero to identify the stacker select number in bits 1 to 3 as belonging to the card in the primary path. This identification is carried along unchanged as the stacker select values are shifted through the stations so that the hopper from which a card originated can be found after the card paths have merged. Bit 4 identifies cards in the secondary path by being permanently set. Bits 5 to 7 represent the stacker number for the secondary card.

Sense Byte 4

Sense byte 4 contains the stacker select numbers for two successive card stations. Bits 0 to 3 represent the stacker designation and the origin of the card in the punch or preprint station, bits 4 to 7 show the designation and origin of the card at the print station, as shown in the following table.

Bit	*Meaning*	*Card Location*
0	primary (0)/secondary (1)	Punch or preprint station
1	binary value 4	
2	binary value 2	
3	binary value 1	
4	primary (0)/secondary (1)	After print station
5	binary value 4	
6	binary value 2	
7	binary value 1	

Bits 0 and 4 are either 0 or 1 depending on whether the card originated in the primary or secondary path. The stacker select number is that which was transferred from the previous station or may be a number that was introduced by a 'punch stacker select' command. The stacker select number assigned to a card that has passed the print station is the final stacker selection for that card and cannot be altered.

Sense Byte 5

Sense byte 5 contains, in bits 0 to 3, the final stacker selection that is placed into the select magnets. Bits 4 to 7 hold the stacker number of the card that was just stacked. The origin of each card is also given, as shown in the following table.

Bit	*Meaning*	*Card Location*
0	primary (0)/secondary (1)	Corner station (to be stacked)
1	4	
2	2	
3	1	
4	primary (0)/secondary (1)	Stacker pocket (was just stacked)
5	4	
6	2	
7	1	

Sense Byte 6

The information in sense byte 6 can identify the first card column in which an invalid card code or column compare check was detected during a read operation, or the first card column in which missing or extra punches were detected during punch operations. Sense byte 6 also indicates that additional invalid information was detected (if this is the case). The bits have the following meanings assigned:

Bit	*Designation*
0	Multi data check
1	Binary value 64
2	Binary value 32
3	Binary value 16
4	Binary value 8
5	Binary value 4
6	Binary value 2
7	Binary value 1

Multi Data Check (Bit 0)

The multi data check bit is set if additional invalid data was detected after the first invalid card column was found. This means that the entire card must be inspected.

Bits 1 to 7

Bits 1 to 7 identify the card column in which the first (possibly the only) error was detected. The column count thus allows pin-point correction. For normal or column binary cards, the count may be any number from 1 to 80.

2560 ERROR RECOVERY

The following paragraphs describe the minimum action the operating system and/or the operator should take to deal with errors or unusual conditions in the 2560 or its front end. Errors or other unusual conditions exist whenever the unit or channel status contains any indication other than channel end, device end, or busy.

Unit Check in CSW

When a unit check occurs, the operating system should at least analyze sense byte 0, but preferably the remaining sense bytes as well. Sense byte 0 will show the major causes of the unit check. The following text describes the suggested recovery procedures for conditions which are indicated by the contents of sense byte 0.

Command Reject (Sense Byte 0, Bit 0)

The most likely reason for the command reject bit being set is a programming error (for a detailed list of such errors, see "2560 Sense Information", "Sense Byte 0"). If the command was rejected due to such an error, the job in progress should be cancelled and the program corrected.

Intervention Required (Sense Byte 0, Bit 1)

If the intervention required bit is set, the operating system should provide a message that advises the operator to observe the indicator lights on the 2560 console and to proceed as described below.

ATTENTION Light On: This indication can be caused by any of the following conditions:

1. Any stacker is full.
2. The chip box is full.
3. The covers are open.
4. The print interlock arm is not locked (especially likely after repositioning of a print head).
5. The hand wheel is engaged.

Any of these conditions must be corrected and the 2560 START key must then be pressed.

PRIMARY HOPPER CHECK or SECONDARY HOPPER CHECK Light On: The operator should remove the cards from the appropriate hopper, repair or replace the bottom card, then reinsert the card deck and press the 2560's START key.

MACHINE CHECK Light: The operator should remove the cards from either or both hoppers and press the 2560's NPRO (non-process runout) key. The operation in progress was not completed and, therefore, requires a restart (new set-up). Sense byte 2 contains a record of the original positions of the cards in the machine; sense byte 1 shows the type of check responsible for the intervention required bit being set; sense bytes 3, 4, and 5 show the stacker select numbers assigned to the cards. The operating system can, therefore, assist the operator in the restart procedure required for the job.

FEED CHECK Light: If a feed check is the cause for the intervention required bit being set, the operating system should provide a message (based on the information in sense byte 1) that tells the operator the area in which a check occurred. The cards must be run out of the machine and a restart must be set up.

Note: After power-on reset, the 2560's FEED CHECK light comes on automatically. This does not indicate an error. The FEED CHECK light is on to remind the operator to press the NPRO key prior to inserting any cards. This precaution ensures proper operating conditions after initial power-on.

Loss of SECONDARY READY or PRIMARY READY Lights: The operator has probably pressed the 2560's STOP key by accident. He should then press the START key to continue. The READY light also goes off when a hopper is empty. In this case, the operator may either reload the empty hopper or simply press the START key; the respective ready light will then go on.

Equipment Check (Sense Byte 0, Bit 3)

If the equipment check bit is set, the operating system should direct the card that has been read or punched into a stacker that has not been assigned for the job in progress. This is because the data read from or punched into that card is unreliable. Whether the entire job must be restarted or not depends on the application program. A message should be issued to the operator advising him to visually check the card and the first failing column (recorded in sense byte 6) and to continue or abandon the job as appropriate. Usually the READ CHECK or PUNCH CHECK light on the 2560's operator panel will be on.

Data Check (Sense Byte 0, Bit 4)

If the data check bit is set, the operating system should analyze the contents of sense byte 6 to find out whether more than one card column is affected and, if not, which column contains the invalid code. For a read operation, the error may be corrected by replacing the affected card by a duplicate card in which the error has been corrected. The operator should therefore run the cards out and restart. However, because the invalid card column has been read into main storage, as a 'blank', it may also be possible to effect on-line correction.

If data check is accompanied by a feed check or machine check, the operating system should ignore the data check and provide a message advising the operator to restart the program.

If data check is set during a punch operation, recovery should be effected by re-issuing the command. This is possible because punching has not actually started and the card has not yet moved. If the repeated command causes another data check, a hardware error is likely. A print operation that causes data check can be retried in the same way.

Feed Check/Machine Check (Sense Byte 0, Bit 5)

If the feed check/machine check bit is set, the operating system should sense the card position image in sense byte 2 and examine the feed failure indications in sense byte 1 to obtain the correct reconfiguration data for a restart. In addition, the stacker select information recorded in sense bytes 3, 4, and 5 should be used to identify the origin of the cards. A message should then be issued to the operator advising him to run out all cards from the 2560, then set up for restart as appropriate. If repeated feed or machine checks occur, the CE must be notified.

No Card Available (Sense Byte 0, Bit 6)

If the no card available bit is set, the operating system should issue a read and feed, punch or punch and feed command to fill the empty punch or preprint station. The failing command can then be repeated successfully.

Channel Data Check in the CSW

If channel data check is set in the CSW, a read operation may have placed incorrect data into main storage. The data has correct parity but may be unreliable. Meanwhile, the buffer load part of a punch or print operation has been completed, but the mechanical part of the operation has not been started. The operating system should therefore retry punch or print operations without issuing any other command because the card is still in the correct physical position in the machine.

Note: If channel data check is found, the operating system should always check whether a limited channel logout exists at storage location 176. This logout shows how far the operation progressed and/or how it was terminated.

Channel Control Check in the CSW

If channel control check is set in the CSW, the operating system should issue an appropriate message to advise the operator to set up the program at a logical point (after it has attempted to retry the operation). Channel control check is usually a severe error associated with parity errors in data addresses, CCW addresses or the contents of the CCW itself. If the error persists, the CE should be notified.
Note: If channel control check is found, the operating system should always check whether a limited channel logout exists at storage location 176. This logout shows how far the operation progressed and/or how it was terminated.

IBM 3203 Printer, Models 1 and 2

This section provides introductory information on the 3203 Printer, Models 1 and 2, and describes the commands, status reports, sense information, and error recovery procedures which apply when the 3203 is under control of the integrated printer attachment.

GENERAL DESCRIPTION

The 3203 is a line printer bolted onto the system frame. It is controlled by an integrated attachment in the CPU and by additional electronic circuitry under the printer covers. If equipped with a 48-character set, a 3203 Model 1 prints at 600 lines per minute (lpm) and the Model 2 prints at 1200 lpm. Both models have 132 print positions and standard line spacings of six or eight lines per inch which can be selected by the operator.

The main functional units of the 3203 are a print hammer unit, an interchangeable print cartridge containing the characters, and a tapeless carriage controlled from the CPU.

On the Model 1, the print hammer unit oscillates so that one hammer can serve two print positions. The hammers are mounted in a movable motor-driven rack. The print positions 1, 3, 5, 7, . . . and 2, 4, 6, 8 . . . are activated alternately. On the Model 2, the print hammer unit is fixed and one hammer serves one print position only.

The 3203 is equipped with the IBM 1416 Interchangeable Train Cartridge which is also used on the IBM 1403 Printer Model N1. The Universal Character Set (UCS) feature is standard.

Forms

The 3203 prints on continuous one- to six-part forms which are punched at the margins. The acceptable sizes are up to 24 in. (610 mm) long and 20 in. (508 mm) wide from edge to edge. To allow adjustment of the column locations in relation to the margins, a forms width not exceeding 17-25/32 in. (452 mm) is recommended. The minimum forms length is 3 in. (76.2 mm) and the minimum width is 3-1/2 in. (89 mm).

Margin-punched cards, preferably of long-grain stock, may also be used. Widths of 8-1/2 in. (216 mm), 14-7/8 in. (378 mm) and 15-7/8 in. (403 mm) are recommended, and there should be two, three, or four cards per fold.

Manual Adjustments

The following manual controls are provided:

1. A forms thickness adjustment to ensure uniform print quality over a variety of forms.
2. A print impression adjustment to adjust the hammer impact for various combinations of forms and ribbons.
3. A knob for adjusting the vertical positioning of the forms.
4. Lateral adjustment of the tractor units for horizontal positioning of the forms.

Operator Panel

The following paragraphs describe the keys, switches, and lights on the 3203's operator panel.

START Key: Pressing the START key places the printer into the ready state, with the printer READY light on. The printer can only operate in the ready state. The START key is ineffective if the INTERLOCK light, the CHECK light, or the FORMS light is on.

STOP Key: When the STOP key is pressed, the printer completes the current operation and stops. The printer is then in the not ready state, a prerequisite for manual operations (loading forms, adjustments, and so on).

CARRIAGE RESTORE Key: Pressing the CARRIAGE RESTORE key causes the forms carriage to advance to print line 1. The line counter (which replaces the conventional carriage tape) in the printer attachment is set to 1. The ribbon drive is activated until one second after the CARRIAGE RESTORE key is released.

The CARRIAGE RESTORE key is operational only when the printer is in the not ready state.

CARRIAGE SPACE Key: Pressing the CARRIAGE SPACE key causes the form to advance one space. The CARRIAGE SPACE key is operational only when the printer is in the not ready state.

Space Select Switch: The space select toggle switch permits the operator to select line spacing at six or eight lines per inch.

Reset Counter Switch: Operating the reset counter switch resets the carriage line counter in the printer attachment to line 1 without moving the forms. When released, the switch automatically returns to the OFF position. The reset counter switch permits the forms and the counter to be synchronized before operation.

The counter reset switch is operational only when the printer is in the not ready state.

INTERLOCK Light: The INTERLOCK light is turned on when the printer's front unit is open. It goes out when the unit is closed and the printer's START key is pressed or a system reset, or system check reset, is performed.

FORMS Light: The FORMS light is turned on when the end of the last form is about 3 in. (76 mm) below the print line or the forms have jammed.

READY Light: The READY light is turned on when the printer's START key is pressed and the INTERLOCK, CHECK, and FORMS lights are off. The READY light is turned off when the printer's STOP key is pressed, or when the INTERLOCK, CHECK or FORMS light comes on.

CHECK Light: The CHECK light is turned on whenever an error condition is detected. Unit check is indicated to the system. Detailed information on the error condition is available in the sense bytes.

3203 COMMANDS

Write Commands

Write commands cause data to be transferred from main storage to the print line buffer; the data transfer is followed by the electro-mechanical print operation, including any carriage motion. The data transfer begins at the storage location designated by the data address (CCW bits 8 to 31) and proceeds in ascending order of address. The data transfer ends either when the print line buffer is filled or when the length count (CCW bits 48 to 63) has been reduced to zero, whichever occurs first. To correspond with the print line width, the count should be 132 (decimal). If the output area contains more characters than appropriate for the print line width or if the count is less than the print line width, incorrect length (bit 41 in the CSW) is indicated unless the SLI flag is on and the CD flag is off in the current CCW. Channel end (bit 36 in the CSW) is indicated when the data transfer from main storage to the print line buffer has been completed. Device end (bit 37 in the CSW) is indicated when the mechanical print operation and any carriage operations have been carried out. Channel end and device end are interruption conditions (but only for the last command if chaining is in progress).

The printer attachment accepts the write commands shown in Figure 60.

Command Code									Command
	CCW Bits								
Hex	0	1	2	3	4	5	6	7	
01	0	0	0	0	0	0	0	1	Write without spacing
09	0	0	0	0	1	0	0	1	Write and space 1 after printing
11	0	0	0	1	0	0	0	1	Write and space 2 after printing
19	0	0	0	1	1	0	0	1	Write and space 3 after printing
89	1	0	0	0	1	0	0	1	Write and skip to channel 1 after printing
91	1	0	0	1	0	0	0	1	Write and skip to channel 2 after printing
99	1	0	0	1	1	0	0	1	Write and skip to channel 3 after printing
A1	1	0	1	0	0	0	0	1	Write and skip to channel 4 after printing
A9	1	0	1	0	1	0	0	1	Write and skip to channel 5 after printing
B1	1	0	1	1	0	0	0	1	Write and skip to channel 6 after printing
B9	1	0	1	1	1	0	0	1	Write and skip to channel 7 after printing
C1	1	1	0	0	0	0	0	1	Write and skip to channel 8 after printing
C9	1	1	0	0	1	0	0	1	Write and skip to channel 9 after printing
D1	1	1	0	1	0	0	0	1	Write and skip to channel 10 after printing
D9	1	1	0	1	1	0	0	1	Write and skip to channel 11 after printing
E1	1	1	1	0	0	0	0	1	Write and skip to channel 12 after printing

Notes:

1. If a write and skip command specifies a channel for which no code exists in the buffer, the carriage does not move and the command ends with unit check set and the no channel found bit (bit 6) set in sense byte 0.
2. If a write and skip command orders the carriage to go to the channel at which it is currently located, the form moves until that channel is detected the next time.

Figure 60. 3203 Write Commands [10839]

Carriage Control Commands

Carriage control commands consist of space and skip commands and the 'load carriage control buffer' command. For space and skip commands, the command code is transferred to the printer attachment, then channel end is indicated in the initial status and the carriage operation is started. Device end is indicated when the mechanical operation is completed at the 3203. Device end is an interruption condition for space and skip commands, unless command chaining is in progress.

Figure 61 shows the space and skip commands available for the 3203.

Carriage Control Buffer Structure

The 3203's carriage is not controlled by paper tape (the method used in the IBM 1403 Printer and other IBM high-speed line printers). Instead, the 3203 employs a 192-byte carriage control buffer.

Each carriage control buffer byte represents one line on the forms sheet; byte 1 represents the first line of a sheet, byte 192 represents the last line of a sheet (assuming the largest possible sheet, which is 24 inches from fold to fold). Each byte may be loaded with a number ranging from 0 to 12 (corresponding to the channel numbers punched in the familiar carriage control paper tape, used on the IBM 1403 Printer and others). The zero represents no channel designation ("no punch"). To designate the actual length of a form (specified on tape-controlled carriages by cutting the control tape to size) an end-of-sheet specification can be set into any byte of the buffer. The buffer byte codes are shown in Figure 62.

The end-of-sheet specification causes the counter (which monitors the position of the carriage) in the printer attachment to wrap around when end-of-sheet is recognized. For information about correct end-of-sheet code placement see "Assigning the End-of-Sheet Code".

Command Code									Command
Hex	CCW Bits 0	1	2	3	4	5	6	7	
0B	0	0	0	0	1	0	1	1	Space 1
13	0	0	0	1	0	0	1	1	Space 2
1B	0	0	0	1	1	0	1	1	Space 3
8B	1	0	0	0	1	0	1	1	Skip to channel 1
93	1	0	0	1	0	0	1	1	Skip to channel 2
9B	1	0	0	1	1	0	1	1	Skip to channel 3
A3	1	0	1	0	0	0	1	1	Skip to channel 4
AB	1	0	1	0	1	0	1	1	Skip to channel 5
B3	1	0	1	1	0	0	1	1	Skip to channel 6
BB	1	0	1	1	1	0	1	1	Skip to channel 7
C3	1	1	0	0	0	0	1	1	Skip to channel 8
CB	1	1	0	0	1	0	1	1	Skip to channel 9
D3	1	1	0	1	0	0	1	1	Skip to channel 10
DB	1	1	0	1	1	0	1	1	Skip to channel 11
E3	1	1	1	0	0	0	1	1	Skip to channel 12

Notes:

1. If a skip command specifies a channel for which no code exists in the buffer, the carriage does not move and the command ends with unit check set in the CSW and the no channel found bit (bit 6) set in sense byte 0.
2. If a skip command orders the carriage to go to the channel at which it is already located, and the preceding command moved the carriage, the carriage does not move and channel end and device end are presented. If the preceding command was a write without space, the carriage moves until the specified channel is detected next time.

Figure 61. 3203 – Carriage Control Space and Skip Commands [10840]

Hex	Buffer Byte Code Bits 0	1	2	3	4	5	6	7	Meaning
00	0	0	0	0	0	0	0	0	No channel (no punch)
01	0	0	0	0	0	0	0	1	Channel 1
02	0	0	0	0	0	0	1	0	Channel 2
03	0	0	0	0	0	0	1	1	Channel 3
04	0	0	0	0	0	1	0	0	Channel 4
05	0	0	0	0	0	1	0	1	Channel 5
06	0	0	0	0	0	1	1	0	Channel 6
07	0	0	0	0	0	1	1	1	Channel 7
08	0	0	0	0	1	0	0	0	Channel 8
09	0	0	0	0	1	0	0	1	Channel 9
0A	0	0	0	0	1	0	1	0	Channel 10
0B	0	0	0	0	1	0	1	1	Channel 11
0C	0	0	0	0	1	1	0	0	Channel 12
0D..FF	0	0	0	1	0	0	0	0	End-of-sheet

Figure 62. 3203 – Carriage Control Buffer Byte Codes [10841]

Assigning the End-of-Sheet Code: The end-of-sheet code must be set into the buffer byte that represents the last printable line of a given sheet. The last printable line of a sheet is determined by multiplying the sheet length (in inches) by the desired line spacing, which can be either six lines or eight lines per inch.

For example: A 12-inch sheet multiplied by eight lines per inch results in 96 printable lines per sheet. The end-of-sheet code must be assigned to line 96 (buffer byte 96). A 12-inch sheet used with six lines per inch spacing results in 72 printable lines per sheet, so the end-of-sheet code must be assigned to line 72. Correct end-of-sheet code assignment ensures that the carriage control buffer remains in synchronism with the form. If the end-of-sheet code is not assigned to the last printable line of a sheet, the control counter wraps around to zero too early, causing information for the next sheet to be printed on the last lines of the previous sheet. There is no error indication to show that the counter is not synchronised with the form.

Load Carriage Control Buffer

The 'load carriage control buffer' command code is:

Hex	CCW Bits 0 1 2 3 4 5 6 7
63	0 1 1 0 0 0 1 1

The 'load carriage control buffer' command transfers data from main storage to the carriage control buffer. The load operation begins at the address specified in bits 8 to 31 of the CCW and proceeds in ascending order of address. The buffer is loaded in ascending order of position until the buffer is filled, or the end-of-sheet code is detected, or the count in CCW bits 48 to 63 is exhausted, whichever occurs first. At that time channel end and device end are presented and the carriage line counter is reset to "first line". First line means that the current carriage position is assumed to represent the first line of the sheet.

If the end-of-sheet code is missing, the carriage line counter is prevented from wrapping at the correct moment, and wraps instead at line 192 plus 1 (this is the default value). Consequently, in cases where the forms length is not 193, the operation is asynchronous. A missing channel 1 code prevents recognition of end-of-forms, suppresses RESTORE key operation (as a safeguard against "carriage runaway") and causes a forms check.

UCS Commands

Universal character set (UCS) commands are always available because the UCS feature is a standard feature of the 3203.

Figure 63 shows the UCS commands available for the 3203.

Command Code									Command
Hex	CCW Bits 0	1	2	3	4	5	6	7	
F3	1	1	1	1	0	0	1	1	Load UCS Buffer with folding
FB	1	1	1	1	1	0	1	1	Load UCS without folding
73	0	1	1	1	0	0	1	1	Block data check
7B	0	1	1	1	1	0	1	1	Allow data check

Figure 63. 3203 UCS Commands [10842]

Load UCS Buffer with Folding

The 'load UCS buffer with folding' command causes data to be transferred from main storage to the UCS buffer. The data transferred represents the chain image. During transfer, the EBCDIC codes of the first, second, and third quadrants of the standard EBCDIC table are "folded" into the fourth quadrant of this table so that four different EBCDIC codes cause one and the same character to be printed. Because the quadrants of the EBCDIC table are identified by bits 0 and 1 of a byte, folding is technically accomplished by suppressing bits 0 and 1 during code comparison so that, effectively, the quadrant specification is ignored.

The data transfer begins at the main storage location specified in bits 8 to 31 of the CCW and proceeds in ascending order of address until the 240-byte UCS buffer is filled or the length count (bits 48 to 63 of the CCW) has been reduced to zero, whichever occurs first. At the end of the data transfer channel end and device end are both indicated. The UCS buffer remains loaded until it is reloaded or power goes off.

Note: The UCS buffer is automatically initiated at IMPL time. The initial data is the standard 48-character set. This set is overwritten by the first UCS buffer load command, and the new UCS data is automatically recorded on the diskette. The backup data on the diskette is used when machine-check situations require that the attachment is reloaded with microprogram.

Load UCS Buffer without Folding

The 'load UCS buffer without folding' command is identical to the 'load UCS buffer with folding' command except that folding does not occur. Only one EBCDIC code corresponds to each print character.

Block Data Check

The 'block data check' command provides the means to suppress data checks that can occur if, for example, the print line buffer contains a character bit pattern that is not available in the UCS buffer.

The 'block data check' command is always available because the 3203 is equipped with the UCS feature. The command causes neither data transfer nor any mechanical operation. Only the command code is transferred, and channel end and device end are both set in the initial status. When 'block data check' is given, data checks are suppressed until an 'allow data check' command is given, power goes off, or a power-on reset occurs.

Note: The 'block data check' command for the 3203 is not subject to any restriction in use. It can be given at any time, and can be included in a command chain.

Allow Data Check

The 'allow data check' resets the effect of a previously-issued 'block data check' command. The 'allow data check' command need only be given to reset a 'block data check' command; if neither command is given, data checks are allowed.

The 'allow data check' command causes neither data transfer nor any mechanical operation. Only the command code is transferred and both channel end and device end are set in the initial status.

Note: The 'allow data check' command can be given at any time, and can be included in a command chain.

Automatic UCS Buffer Initialization/Reloading

The UCS buffer is automatically loaded with a standard 48-character set at IMPL time, enabling the 3203 to operate even if no chain image is loaded. Any load UCS buffer command overwrites the initial value and the new pattern is at the same time recorded on the diskette. In case of processor damage, the UCS buffer is automatically reloaded from the diskette so that the pattern last used is available.

Control No-Op Command

The 'control no-op' command (command code 00000011) performs no function in the 3203. When this command is given, channel end, device end, and any other status conditions that exist at the time are indicated in the initial status.

Read Commands

No 'read' command is available for the 3203. A 'read' command issued to the printer is rejected.

Sense Command

The 'sense' command is usually given when unit check has been set in the CSW, and provides a means of transferring up to six bytes of sense information from the printer attachment to main storage. The sense bytes contain information about errors or unusual conditions in the printer or its controlling front end; the operating system analyzes this information before taking appropriate action to recover from the error(s). The 'sense' command code is:

Hex	*CCW Bits* *0 1 2 3 4 5 6 7*
04	0 0 0 0 0 1 0 0

The sense information is stored into the main storage location specified by CCW bits 8 to 31, in ascending order of address. The number of sense bytes to be transferred is specified in CCW bits 48 to 63. Channel end and device end are both set when the transfer of sense information to main storage is completed.

For details of the information that can be obtained by use of the 'sense' command, see "3203 Sense Information" in this section.

3203 STATUS INFORMATION

The following text gives the meanings of the status indications which are given in response to 3203 commands.

Unit Status

The unit status is indicated in bits 32 to 39 of the CSW. The unit status is directly related to a command that has been given to, completed by, or terminated by the 3203. The bits are assigned the following meanings:

Bit	*Designation*
32	Attention (not used)
33	Status modifier (not used)
34	Control unit end (not used)
35	Busy
36	Channel end
37	Device end
38	Unit check
39	Unit exception

Attention (Bit 32)

The attention bit is not used.

Status Modifier (Bit 33)

The status modifier bit is not used.

Control Unit End (Bit 34)

The control unit end bit is not used.

Busy (Bit 35)

The busy bit, when set, indicates that the printer and its controlling front end logic are occupied with executing some previously-initiated operation.

Channel End (Bit 36)

The channel end bit, when set, indicates that the data transfer part of a 3203 command, or the transfer of the command code, is completed.

Device End (Bit 37)

The device end bit, when set, indicates that the 3203 has completed the mechanical portion (if any) of an operation. Device end thus signals that the printer is free to accept and execute a new command. Device end is set alone when the printer is manually transferred from the not-ready to the ready state (when the printer's START key is pressed).

Unit Check (Bit 38)

The unit check bit is set for various errors or other unusual conditions that may have occurred in the 3203 and/or its controlling front end logic. Because the setting of unit check does not define the error condition, a 'sense' command should be issued to the 3203. The contents of the sense bytes will show the actual cause of unit check being set. For details of the conditions that can cause unit check to be set, see "3203 Sense Information" in this section.

The setting of unit check breaks command chaining.

Unit Exception (Bit 39)

The meaning of the unit exception indication depends on the command during whose execution the bit was set.

If unit exception is set during execution of a *'load carriage control buffer' command,* the channel 1 code is missing. This indicates that forms control is incorrect (or absent) and the RESTORE key is not operational.

If unit exception is set during execution of a *command causing carriage motion* a channel 12 code has been detected during a space operation. The meaning of channel 12 is assigned by the programmer.

Channel Status

The channel status information is recorded in bits 40 to 47 of the CSW; the bits have the following meanings assigned:

Bit	*Designation*
40	Program-controlled interruption
41	Incorrect length
42	Program check
43	Protection check
44	Channel data check
45	Channel control check
46	Interface control check (not used)
47	Chaining check (not used)

The channel status bits have the same standard functions for the 3203 as for any other device attached via a channel, integrated adapter, or integrated attachment. These functions are described for the 2560 under "2560 Status Information" in the section "IBM 2560 Multi-function Card Machine; Models A1 and A2". For a more detailed description of the channel status bits, see *IBM System/370 Principles of Operation,* GA22-7000.

Note: A set PCI flag bit in the first CCW after a 'start I/O' instruction is not recognized if the 'start I/O' instruction finds the 3203 is not available.

3203 SENSE INFORMATION

Sense Byte 0

The bits in sense byte 0 have the following meanings assigned:

Bit	*Designation*
0	Command reject
1	Intervention required
2	Bus out check (not used)
3	Equipment check
4	Data check
5	Chain buffer parity check
6	No channel found
7	Channel 9

Command Reject (Bit 0)

The command reject bit, when set, indicates that the current command was rejected because it was not assigned to the 3203. A read command being issued causes command rejection. The fact that the current command has been rejected is indicated by *unit check* being set in the initial status. Setting of unit check causes chaining (if specified) to be suppressed.

Intervention Required (Bit 1)

The intervention required bit, when set, indicates that operator intervention is necessary because the 3203 has lost the ready state. The ready state is lost in the following situations:

1. The 3203's STOP key is pressed.
2. The train gate is open (cartridge not properly seated).
3. A forms jam has occurred (switching on the CHECK light).
4. The forms have run out (switching on the FORMS light).
5. A carriage sync check has occurred (switching on the CHECK light).
6. A chain sync check has occurred (switching on the CHECK light).
7. A hammer driver could not be reset, or the CE hammer-on check switch was accidentally operated, causing the coil protect bit (bit 2, sense byte 2) to be set.
8. The hammer bar did not shift (3203 Model 1 only).
9. The check circuitry is defective (this sets the any-hammer-on check bit, and also forces the coil protect check bit, in sense byte 2).
10. An error occurred in the subscan counter, setting the subscan ring check bit in sense byte 2.
11. A chain buffer address register check has occurred, setting the bit of the same name in sense byte 2.

The setting of the intervention required bit causes *unit check* to be set in the CSW at the initiation of a 'start I/O' or 'test I/O' instruction or at device end time, depending on when the condition arises. Intervention required is reset when the printer is restored to the ready state.

Bus Out Check (Bit 2)

The bus out check bit is not used.

Equipment Check (Bit 3)

This bit indicates a program-correctable error that occurred in the 3203 or the front end logic. The error is corrected the next time the printer is selected for a 'start I/O', 'halt I/O', or 'halt device' instruction.

The equipment check bit is set by one or more of the nine error conditions which are represented by the bits of sense bytes 4 and 5. For details of these conditions, see "Sense Byte 4" and "Sense Byte 5" in this section.

The detection of an equipment check causes unit check to be set at the time device end (with or without channel end) is set.

Note: Setting of the equipment check bit does not cause the 3203 to lose the ready state.

Data Check (Bit 4)

The data check bit can only be set when data checks are not prevented by a 'block data check' command. Data check will then be set if the print line buffer contains a character pattern for which no matching pattern is found in the UCS buffer during a UCS print operation. This is usually due to a wrong program being used.

The fact that data check is set is indicated by unit check being set in the CSW at device end time.

Chain Buffer Parity Check (Bit 5)

The chain buffer parity check bit is set to indicate a chain buffer parity error. The presence of a chain buffer parity check causes unit check to be set at channel end time.

No Channel Found (Bit 6)

The no channel found bit is set when a skip command or a write and skip command did not find the channel code (in the carriage control buffer) to which the carriage was to advance. The setting of the no channel found bit causes unit check to be set at device end time.

Channel 9 (Bit 7)

The channel 9 bit, when set, indicates that a channel 9 code was detected in the carriage control buffer during the execution of a space command or a write and space command. The same situation when caused by a manual space or any of the skip commands does not set the channel 9 bit. The setting of the channel 9 bit causes unit check to be set at device end time.

Sense Byte 1

Sense byte 1 is not used.

Sense Byte 2

The bits in sense byte 2 represent eight conditions, any of which can cause the 3203 to lose its ready state. The setting of one of these bits causes the intervention required bit to be set in sense byte 0. The bits in sense byte 2 have the following meanings assigned:

Bit	*Designation*
0	Interlock (chain gate open)
1	Forms check (jam)
2	Coil protect check
3	Subscan ring check
4	Chain buffer address register check
5	Hammer unit shift check (applies to 3203 Model 1 only
6	Any-hammer-on check
7	Device ready check

Interlock (Bit 0)

The interlock bit is set to indicate that a chain gate is open, or that the lock lever is not closed.

Forms Check (Bit 1)

The forms check bit, when set, indicates a paper jam.

Coil Protect Check (Bit 2)

The coil protect check bit, when set, indicates that power was removed from the hammer circuits to prevent damage to the hammer coils.

Subscan Ring Check (Bit 3)

The subscan ring check bit is set if there is an error in the subscan ring counter (hardware) or a drum emitter failure.

Chain Buffer Address Register Check (Bit 4)

This bit is set to indicate that there is a loss of synchronism between the chain position and chain buffer addressing at home pulse time (at this time, both should be in step).

Hammer Unit Shift Check (Bit 5)

The hammer unit shift check bit, when set, indicates a shift failure due to a malfunction of the linear motor. This bit is only used for a 3203 Model 1.

Any-Hammer-On Check (Bit 6)

The any-hammer-on check bit is set to show that protection of the hammer coils is no longer possible because of a failure in the coil protect monitoring circuits. This bit can also mean that the 'any-hammer-on' latch was not turned off, because a hammer failed to fire.

Device Ready Check (Bit 7)

The device ready check bit, when set, indicates that the ready state could not be achieved because the chain motor was not up to speed or the carriage motor rotation was in an undefined position.

Sense Byte 3

The bits in sense byte 3 represent three types of error associated with carriage control. The setting of one of these bits causes the intervention required bit to be set in sense byte 0. The bits in sense byte 3 have the following meanings assigned:

Bit	*Designation*
0	(Not used)
1	(Not used)
2	(Not used)
3	Carriage inhibit check
4	(Not used)
5	(Not used)
6	Step check
7	Move check

Carriage Inhibit Check (Bit 3)

The carriage inhibit check bit, when set, indicates that the inhibit pulses which should be sent to a halted carriage are failing, or that the 'inhibit' line is damaged.

Step Check (Bit 6)

The step check bit, when set, indicates that the carriage motor's photo emitter is producing the wrong numbers of feedback or check pulses, or that the phase propagation for the stepper motor is defective.

Move Check (Bit 7)

The move check bit, when set, indicates that the carriage either failed to move or moved too slowly.

Sense Byte 4

The bits in sense byte 4 represent eight error conditions, any one of which can cause the equipment check bit to be set in sense byte 0. An equipment check caused by a condition in sense byte 4 is a program-correctable error.

Bit	*Designation*
0	Hammer reset failure check
1	No fire check
2	Misfire check
3	Print data buffer parity check
4	Check bit buffer parity check
5	Chain buffer parity check
6	Buffer address register check
7	Clock check

Hammer Reset Failure Check (Bit 0)

This bit, when set, indicates that a hammer driver failed to reset when addressed for resetting.

No Fire Check (Bit 1)

The no fire check bit, when set, indicates that a hammer failed to fire when addressed for firing.

Misfire Check (Bit 2)

The misfire check bit, when set, indicates that a hammer fired without being addressed.

Buffer Parity Checks (Bits 3, 4, and 5)

The buffer parity check bits for the print data buffer, check bit buffer and chain buffer are set to indicate parity errors in the buffers concerned.

Buffer Address Register Check (Bit 6)

The buffer address register check bit is set when an addressing error causes a subscan to seem excessively long.

Clock Check (Bit 7)

The clock check bit is set when extra clock steps (possibly due to "noise") are detected.

Sense Byte 5

Bit 0 in sense byte 5 represents one further error condition (in addition to those in sense byte 4) which, when set, causes the equipment check bit to be set in sense byte 0. This equipment check is a program-correctable error.

Bit	*Designation*
0	Open coil check
1	(Not used)
2	(Not used)
3	(Not used)
4	(Not used)
5	(Not used)
6	(Not used)
7	(Not used)

Open Coil Check (Bit 0)

The open coil check bit, when set, indicates that a lack of continuity was detected through one of the hammer coils.

3203 ERROR RECOVERY

The following text describes the minimum action the operating system should take to deal with errors or other unusual conditions that may occur. Errors and other unusual conditions are usually indicated by the setting of unit check or any of the other status bits (except an end condition or busy) in the CSW.

Unit Check in CSW

When a command ends with unit check set in the CSW, the operating system should issue a 'sense' command and subsequently inspect at least sense byte 0 to find the reason for the unit check. The following text describes the suggested error recovery procedures for errors shown by bits set in sense byte 0.

Command Reject (Sense Byte 0, Bit 0)

The most likely cause of command reject being set is that a 'read' command has been issued. The operating system should trace back the program and provide a message advising the system programmer to correct the error.

Intervention Required (Sense Byte 0, Bit 1)

If the intervention required bit is set, the printer has lost its ready state and manual intervention is required. The operating system should analyze sense bytes 2 and 3 because these bytes contain error information not indicated by the 3203's indicator lights. If sense bytes 2 and 3 show the cause of the error, an appropriate message should then be issued to the operator advising him of the error and requesting him to press the printer's START key (to restore the ready state).

If the error is not obvious from the information in sense bytes 2 and 3, the message should advise the operator to check the indicator lights on the 3203 operator panel. These lights, as described below, can suggest the reason for the printer losing its ready state.

INTERLOCK Light On: The operator should close the train gate and make certain the lock lever is fully engaged. If this does not correct the error, the CE should be notified..

FORMS Light On: The operator should check whether new forms must be inserted. In case of end-of-forms, the printer continues printing and the FORMS light is switched on when the channel 1 code is found in the buffer. The operator must then insert new forms and press the 3203's START key. (The end-of-forms feelers must be set into their cutouts, otherwise the FORMS light remains on).

CHECK Light on: An error has occurred either in the 3203 or in the front end. Errors in the printer can be conditions such as a forms jam, a chain sync check, any-hammer-on check, a carriage sync check, and so on.

Hardware malfunctions of this type may be overcome by pressing the 3203's START key. However, in case of repeated hardware errors, CE attention is required.

Errors in the printer front end may be checks such as subscan-ring check, chain buffer address register check, coil protect check, and so on. In any such case, the operating system should issue an appropriate message (based on the information in sense bytes 2 and 3) which advises the operator to restore the ready state by pressing the printer START key. The program should repeat the last operation or restart at a logical point. If errors that cause the CHECK light to go on persist, the CE should be notified.

In the case of a carriage step check, the operator should check whether manual carriage operations (single space, restore) can be performed. If they can be performed, the operation should be set up again, otherwise the CE should be notified.

Equipment Check (Sense Byte 0, Bit 3)

If the equipment check bit is set, the operating system should analyze the data provided by sense bytes 4 and 5, and issue a message to the operator advising him of the condition. The program should then retry the last command or display the last print line on the video display. Equipment check conditions are not usually so severe that a retry would be ineffective. However, if equipment check persists, the CE should be notified.

Data Check (Sense Byte 0, Bit 4)

If the data check bit is set, the print pattern sent to the 3203 cannot be printed with the train cartridge currently fitted. In this case, the train cartridge should be changed and the job should be repeated.

Chain Buffer Parity Check (Sense Byte 0, Bit 5)

If the chain buffer parity check bit is set, the operating system should display the last line to be printed and repeat the operation. If the error persists, the CE should be notified.

No Channel Found (Sense Byte 0, Bit 6)

If the no channel found bit is set, the carriage control buffer has been loaded with information that is not appropriate for the current program. The operating system should either reload the carriage buffer or issue a message that indicates what type of control information should be loaded. The operator may also be advised to check the forms on the printer to determine which control program is required.

Channel 9 (Sense Byte 0, Bit 7)

If the channel 9 bit is set, the operating system should take the appropriate action, depending on the use and meaning of channel 9. Setting of the channel 9 bit may indicate a programming error such as the wrong carriage control information for the current program.

Unit Exception in CSW

If the unit exception bit is set, a channel 12 code was detected during spacing and interpretation depends on the meaning which the programmer has assigned to channel 12.

Channel Data Check in CSW

The channel data check bit is usually set as a result of a parity error in the data transferred (such as in a buffer load operation) between main storage and the printer attachment. The error is not severe because the parity has been corrected. The output at the printer is, however, unreliable and the operating system should either retry the operation or use the video screen to display the contents of the output area as it should have been printed. Retry should in any case be attempted. Repeated channel data checks require CE attention.

Note: If channel data check is set, the operating system should analyze storage location 176, which contains the limited channel logout. This logout shows how far the operation progressed and/or how it was terminated.

Channel Control Check in CSW

If the channel control check bit is set, the operation was either terminated or not started due to a severe error in the Model 115's main storage controller or internal bus system. Retry should be attempted and, if unsuccessful, the CE should be notified.

Note: If channel control check is set, the operating system should analyze storage location 176, which contains the limited channel logout. This logout shows how far the operation progressed and/or how it was terminated.

IBM 3340 Disk Storage, Models B1 and B2; IBM 3340 Disk Storage and Control Model A2

This section describes the commands, data formats, status reports, sense information, and error recovery procedures for the 3340 Disk Storage, Models B1 and B2, and the 3340 Disk Storage and Control Model A2 when under control of the direct disk attachment. A 3340 installation used with the Model 115 can consist of two, three, or four disk drives. The prerequisite Model A2 contains two disk drives and a control unit. One or two more drives can be added by attaching a 3340 Model B1 (one drive) or a 3340 Model B2 (two drives).

The characteristics of the IBM 3348 Data Modules used on the 3340 are shown in Figure 64.

	Model of Data Module	
	3348-35	3348-70
Cylinders per data module	348	696
Tracks per cylinder	12	12
Bytes per track	8,368	8,368
Bytes per cylinder	100,416	100,416
Bytes per module	39,944,768	69,889,536

Figure 64. Characteristics of 3348 Data Modules [10843]

The 3348 Data Modules listed in Figure 64 can be used on any 3340. It is possible to change the drive capacity by changing the data module. The online storage capacity of a 3340 installation can thus vary from approximately 70 megabytes (2 drives with 3348-35 data modules) to approximately 280 megabytes (4 drives with 3348-70 data modules).

The data modules are initialized at the IBM plant. During a surface analysis the home addresses, and the eight-byte track descriptions in each record zero, are written. If a skippable defect is found on a track, the corresponding skip displacement bytes (see Figure 67) are written in the home address. During subsequent operations these bytes are used by the control unit to skip the defect. If the data areas of the modules become defective during service, an IBM utility program can be used to flag defective tracks and assign alternate tracks.

All 3340 models have an average access time of 25 ms, an average rotational delay of 10.1 ms, and a nominal read/write rate of 885,000 bytes per second.

3340 Commands

Figure 65 shows the commands which are available for the 3340.

Read Commands

Read commands are used to transfer information from the disk drives to main storage. 'Read data', 'read key and data', and 'read count key and data' commands can be executed in a special record overflow mode. All read commands except 'read initial program load' and 'read sector' can be executed in a special multi-track mode (see Figure 65).

Record overflow mode allows the processing of records which extend from one track to the next. Such records are known as overflow records. To indicate this overflow, the 'write special count, key and data' command is provided, which formats an overflow record segment with bit 4 set in the flag byte (see Figures 67 and 68). Whenever a read or *non-formatting* write command processes the data field of a flagged record, the operation is not terminated at the end of the data field but continues at the data field of record one on the following track. If this record is also flagged, the operation again continues onto the next track. If the advancing read/write head encounters an unusual condition or is inhibited by the file mask, the operation incomplete bit (sense byte 1, bit 7) is set.

The second special mode in which read commands (except 'read initial program load' and 'read sector') can be executed is multi-track mode. Multi-track mode can be set only when read or search commands are given. It is switched on when bit 0 of the CCW is set, causing the control unit to select automatically the read/write head with the next sequential number. This switching of heads takes place at the index point if bit 0 is set and if the data transfer specified in the command has not been initiated.

Read Data

The 'read data' command causes the contents of the data area of a record (see Figure 67) to be transferred to main storage. The data to be read is either:

1. The data area of the record following the next count area (excluding record zero – the track description record) encountered on the track, or
2. The data area of the record encountered when a 'read data' command is chained from a 'read count' or search command (other than 'search home address').

A parity bit is added to each byte of data sent to the direct disk attachment and the validity of the information read is verified. The next command in the chain is then read out, or, if the chain has been completely executed, channel end and device end are presented. If data overrun or data check is detected, the disk attachment retries the command, and if the retry is unsuccessful, channel end, device end, and unit check are set. The data in the key area is not checked during a 'read data' command.

Command Code				Operation	Type
Single Track		Multi-track			
Hex	*CCW Bits 01234567*	*Hex*	*CCW Bits 01234567*		
06	00000110	86	10000110	Read data	Read
0E	00001110	8E	10001110	Read key and data	
1E	00011110	9E	10011110	Read count, key and data	
16	00010110	96	10010110	Read record zero	
12	00010010	92	10010010	Read count	
1A	00011010	9A	10011010	Read home address	
02	00000010			Read initial program load	
22	00100010			Read sector	
05	00000101			Write data	Write
0D	00001101			Write key and data	
1D	00011101			Write count, key and data	
01	00000001			Write special count, key and data	
15	00010101			Write record zero	
19	00011001			Write home address	
11	00010001			Erase	
39	00111001	B9	10111001	Search home address equal	Search
31	00110001	B1	10110001	Search identifier equal	
51	01010001	D1	11010001	Search identifier high	
71	01110001	F1	11110001	Search identifier equal or high	
29	00101001	A9	10101001	Search key equal	
49	01001001	C9	11001001	Search key high	
69	01101001	E9	11101001	Search key equal or high	
04	00000100			Sense I/O	Sense
A4	10010100			Read buffered log*	
03	00000011			No-operation	Control
07	00000111			Seek	
0B	00001011			Seek cylinder	
1B	00011011			Seek head	
0F	00001111			Space count	
13	00010011			Recalibrate	
17	00010111			Restore	
1F	00011111			Set file mask	
23	00100011			Set sector	

* The 'read buffered log' command does not reset the buffered log information. This is done by the "save usage counters" manual operation.

Figure 65. 3340 Commands [10844]

A 'read data' command is executed whether or not it is preceded by any other command.

Read Key and Data

The 'read key and data' command causes the contents of the key and data areas of a record to be transferred to main storage. The key and data to be read are either:

1. The key and data areas of the record following the next count area (excluding record zero) to be encountered on the track, or
2. The key and data areas of a record encountered, when a 'read key and data' command is chained from a 'read count' command or from a search identifier command.

If the key length is zero, the 'read key and data' command is executed like a 'read data' command.

A parity bit is added to each byte of data sent to the direct disk attachment and the validity of the information read is verified. The next command in the chain is then read out, or, if the chain has been completely executed, channel end and device end are presented. If a data overrun, command overrun, or data check is detected, the disk attachment retries the command, and if the retry is unsuccessful, channel end, device end, and unit check are set.

A 'read key and data' command is executed whether or not it is preceded by any other command.

Read Count, Key and Data

The 'read count, key and data' command causes all areas (that is, count, key and data) of the next following record,

excluding record zero, to be transferred to main storage. A parity bit is added to each byte of data sent to the disk attachment and the validity of the information is verified. The next command in the chain is then read out, or, if the chain has been completely executed, channel end and device end are presented. A 'read count, key and data' command is executed whether or not it is preceded by any other command.

Read Record Zero

Record zero is the track description record. A 'read record zero' command causes the count, key, and data areas of record zero to be transferred to main storage. The attachment searches for the index point, counts over gap one, the home address, and gap two, and transfers the data from record zero. A 'read record zero' command chained from a 'search home address' or 'read home address' command is executed immediately and does not cause a search for the index point. After data transfer begins, the 'read record zero' command is processed in the same way as a 'read count, key and data' command.

A 'read record zero' command is executed whether or not it is preceded by another command.

Read Count

A 'read count' command causes the eight bytes of the next following count area (excluding record zero) to be transferred to main storage. A parity bit is added to each byte of data sent to the disk attachment, and the validity of the information is verified. The next command in the chain is then read out, or, if the chain has been completely executed, channel end and device end are presented. If data overrun, command overrun, or data check is detected, the attachment retries the command, and if the retry is unsuccessful, channel end, device end, and unit check are set.

A 'read count' command is executed whether or not it is preceded by another command.

Read Home Address

The 'read home address' command causes five bytes of the home address area, consisting of a one-byte flag, a two-byte cylinder number, and a two-byte head number, to be transferred to main storage. A parity bit is added to each byte of data sent to the disk attachment, and the validity of the information is verified. The next command in the chain is then read out, or, if the chain has been completely executed, channel end and device end are presented. If data overrun or data check is detected, the disk attachment retries the command, and if the retry is unsuccessful, channel end, device end, and unit check are set.

A 'read home address' command is executed whether or not it is preceded by another command.

Read Initial Program Load

The 'read IPL' command causes the disk attachment to seek cylinder zero and head zero, and read the data area of record one. After data transfer begins, the command is executed in the same way as a 'read data' command. A 'read IPL' command must not be preceded by a 'set file mask' command in a chain otherwise the 'read IPL' command is rejected, and unit check is set in the initial status.

Read Sector

The 'read sector' command causes one byte to be transferred from the disk attachment to main storage. The byte contains information needed by a subsequent 'set sector' command during access to data.

The contents of the transferred byte represent the sector number needed for access to the last record processed on the drive, unless the execution of a seek command, a 'set sector' command, a disk storage power-on sequence, or a system reset has intervened. In these cases, an all-zeros byte is transferred. If the last record was processed as an overflow record, the sector number transferred is that of the first segment.

The execution of a 'read sector' command resets orientation information in the disk attachment.

Note: If the rotational position sensing feature is not present, the value 00 (hexadecimal) is transferred to main storage.

Non-formatting Write Commands

Non-formatting write commands cause data to be transferred from main storage to a disk drive. They are used to update existing records, including overflow records.

Write Data

The 'write data' command is normally given for updating the data area of a record. The command causes the specified data to be transferred from main storage to a disk drive. The data transfer continues until the length count specified in the count area of the record has reached zero. The data is then verified, and the next command in the chain is read out, or, if the chain has been completely executed, channel end and device end are presented.

If the 'write data' command is not chained from a 'search identifier equal' command, or a 'search key equal' command in which the comparison of all bytes of the search field on the track gives an equal result, the command is rejected and unit check is set.

If the CCW count is less than specified in the data area length field of the count area, zeros are written in the remainder of the data area.

Write Key and Data

The 'write key and data' command is normally given for writing on the key and data areas of a record. The command is executed like a 'write data' command except that the key area is also updated. If the key area length specified in the count field is zero, the 'write key and data' command has the same effect as the 'write data' command.

If the 'write key and data' command is not chained from a 'search identifier equal' command in which the comparison of all five bytes of the search field gives an equal result, the command is rejected.

Formatting Write Commands

Formatting write commands cause data to be transferred from main storage to a disk drive. The commands are used to initialize tracks and records, and define the lengths of the areas in each record.

Certain clearly defined conditions must exist when formatting write commands are given, otherwise the commands are not executed. These conditions, some of which apply to command chaining, are stated in the following command descriptions.

After the last formatting write command in a chain has been executed, the remainder of the track is erased. If a command of another type is chained from a formatting write command, it is executed after the erasure has taken place. If data overrun occurs during a formatting write operation, the disk attachment writes valid zeros from the time of its detection to the end of the record.

Before reading the following descriptions of formatting write commands, it may be useful to refer to the disk record format shown in Figure 67.

Write Home Address

The 'write home address' command causes seven bytes (the two skip displacement bytes, the flag byte, two cylinder number bytes and two head number bytes) to be transferred from main storage to a disk drive. The first three bytes are generated by the disk attachment. Bit 6 of the flag byte (byte 3) must be set, thus indicating that the track is defective: if bit 6 is zero the command is not executed, and channel end, device end, and unit check are set in the final status. The command reject bit (sense byte 0, bit 0) is also set.

If bit 6 of the flag byte is set, the skip displacement bytes are examined. If they have a bit configuration which indicates a defect in the normal home address area, a gap G1 of 235 bytes is written. If both skip displacement bytes contain all zeros, however, a gap G1 of 107 bytes is written. If the skip displacement bytes show a defect in the count area of the normal record zero, bit 0 of the flag byte in the home address is set before the 'write home address' command is executed.

If the file mask prerequisites are satisfied, the disk attachment selects the index point, writes gap G1, the two physical address bytes, the seven bytes transferred from main storage, and seven detection code bytes. The next command in the chain is then read out, or, if the chain has been completely executed, channel end and device end are presented.

If the byte count in bits 48 to 63 of the CCW is less than three, the 'write home address' command is rejected. If the byte count is more than two but less than seven, the disk attachment provides valid zeros until seven bytes have been written. If the byte count is greater than seven, only the first seven bytes are written.

Write Record Zero

The 'write record zero' command causes data (the track description record) to be transferred from main storage and written on a disk, following the home address area. The first eight bytes from main storage are written in the count area. (The flag byte, the physical address bytes and the skip displacement bytes do not come from main storage but are generated by the disk attachment.) The rest of the data from main storage is written in the key area and the data area, as specified by the respective length counts in the count area. The detection code is written at the end of each field. After such a code has been written for the data area, the disk attachment reads out the next command, or, if the chain has been completely executed, channel end and device end are presented.

The amount of data transferred from main storage to the disk drive never exceeds eight bytes plus the number of bytes specified in the key length and the data length. If the CCW count is less than this total, the disk attachment writes valid zeros in the remainder of the record.

The 'write record zero' command is rejected if it is not chained from a 'write home address' command or a 'search home address' command whose argument was equal to the four bytes (the two cylinder number bytes and the two head number bytes) of the home address area.

Write Count, Key and Data

The 'write count, key and data' command causes a complete record (the count area, key area, and data area) to be transferred from main storage to a disk drive. The first eight bytes from main storage (the flag byte is generated by the disk attachment) are written in the count area. The rest of the data from main storage is written in the key area and the data area, as specified by the respective length counts in the count area. The detection code bytes are written at the end of each area. After writing such bytes for the data area, the disk attachment reads out the next command, or, if the chain has been completely executed, channel end and device end are presented.

The data transferred from main storage to the disk drive never exceeds eight bytes plus the number of bytes

specified in the key length and the data length: if the CCW count is less than this total, the disk attachment writes valid zeros in the remainder of the record.

The 'write count, key and data' command must be chained from a 'write record zero' command, a 'write count, key and data' command, or from a 'search identifier equal' or 'search key equal' command in which the comparison of all bytes of the search field on the track gives an equal result. (A 'read data' command or a 'read key and data' command may be inserted between the search command and the 'write count, key and data' command.) If these rules are not followed, the command is rejected.

Write Special Count, Key and Data

The 'write special count, key and data' command has the same effect as the 'write count, key and data' command, except that the disk attachment sets flag bit 4 to indicate an overflow record segment. The command is used to format overflow record segments.

If any write command except 'write home address' is chained to a 'write special count, key and data' command the command reject bit will be set.

Erase

The 'erase' command has the same effect as the 'write count, key and data' command, except that the disk attachment erases the rest of the track.

Data is transferred from main storage but is not written on the disk. If any write command except 'write home address' is chained to an 'erase' command, the command reject bit is set.

Search Commands

Search commands are issued to find information previously written on the disk storage drive. During search operations, the main storage controller works in write mode, and the disk drive works in read mode. The disk attachment compares the information coming from main storage with that coming from the disk drive.

Each search command operates on one record only: for a subsequent record the search command must be reissued. When the search condition is satisfied, the disk attachment sets an internal status modifier bit, which causes the next command to be skipped. Thus, the successful search operation is used to continue with the channel program.

The following command chain is an example of this procedure:

Command Chain	*Function*
Search key equal	Compares the key with the search argument.
Transfer in channel * – 8	Returns to the search command if searching was unsuccessful.
Read data	Reads the data area if the status modifier was set by a successful search operation.

The 'transfer in channel' command causes the search operation to be repeated until it is successful. After the successful search, the 'transfer in channel' command is skipped and the 'read data' command is executed.

If a search command is the last in a chain and a successful comparison occurs at the first attempt, channel end, device end, and the status modifier are present in the ending status. If the comparison is unsuccessful, only channel end and device end are present.

If a search command is *not* the last in a chain, and a successful comparison occurs, the following command is skipped. If the skipped command is the last in a chain, only channel end and device end are present in the ending status. If the comparison is unsuccessful, the next command is executed.

Search commands may be executed in either single-track or multi-track mode, depending on the state of bit 0 in the CCW (Figure 65).

Search Home Address Equal

The 'search home address equal' command causes the disk attachment to search until the index point is found, then to compare the four bytes of the home address (cylinder and head) coming from main storage with the equivalent four bytes coming from the disk drive. The flag byte is not transferred or compared during a 'search home address equal' command.

If the length count in the CCW exceeds four bytes, the search operation is completed when the four bytes have been received by the disk attachment. A successful comparison causes the next command to be skipped. If the length count in the CCW is less than four bytes, the comparison between the data coming from main storage and the data coming from the drive continues only for the number of bytes specified. If the search conditions of this short field are satisfied, the next command is skipped.

If a bus out parity error is detected during the search operation, unit check, channel end and device end are generated.

A 'search home address equal' command is executed whether or not it is preceded by another command.

Search Identifier Equal

The 'search identifier equal' command causes a comparison to be made to establish if the five bytes of data coming from main storage are equal to the five-byte identifier (cylinder, head and record numbers) coming from the disk drive. The identifier searched is from the next record on the track, record zero included.

If the multi-track bit (CCW bit 1) is zero, only one track is searched. As long as the chained command is reissued, the search continues until the search condition has been satisfied. If this does not occur before two index points have been sensed, unit check and the no record found bit

(sense byte 1, bit 4) are set, and the channel end and device end signals are generated.

If the multi-track bit is set, the head number is incremented by one each time the index point is sensed and, so long as the command is repeated, the search continues until the head number has reached 12. This condition causes unit check and the end of cylinder bit (sense byte 1, bit 2) to be set.

If the length count in the CCW exceeds five bytes, the search operation ends when five bytes have been compared. A successful comparison causes the next command to be skipped. If the length count in the CCW is less than five bytes, the comparison between the data coming from main storage and the data coming from the disk drive continues only for the number of bytes specified. If the search conditions of this short field are satisfied, the next command is skipped.

If a bus out parity error is detected during the search operation, unit check, channel end and device end are generated.

A 'search identifier equal' command is executed whether or not it is preceded by another command.

Search Identifier High

The 'search identifier high' command has a similar effect to the 'search identifier equal' command except that the criterion of comparison is whether the identifier received from the disk drive is higher than the identifier received from main storage.

Search Identifier Equal or High

The 'search identifier equal or high' command has a similar effect to the 'search identifier equal' command except that the comparison determines whether the identifier received from the disk drive is equal to or higher than the identifier received from main storage.

Search Key Equal

The 'search key equal' command causes a comparison to be made, to establish if the bytes of data coming from main storage are equal to the key area bytes coming from the disk drive. The key searched is that of the next record, excluding record zero, unless the 'search key equal' command is chained from a 'read count' command or a 'search identifier' command. In these cases, the key searched is the one in the record whose identifier was read or searched. The 'search key equal' command is executed on the key of record zero only if an immediately preceding search identifier command was executed on the count of record zero. If the comparison is successful, the next command is skipped. If the comparison is unsuccessful or the record has no key, the next command is executed.

If the multi-track bit is zero, only one track is searched. As long as the chained command is reissued, the search continues until the search condition has been satisfied. If this does not occur before two index points have been sensed, unit check and the no record found bit (sense byte 1, bit 4) are set, and the channel end and device end signals are generated.

If the multi-track bit is set, the head number is incremented by one each time the index point is sensed, and, so long as the command is repeated, the search continues until the head number has reached 12. This condition causes unit check and the end of cylinder bit (sense byte 1, bit 2) to be set.

If the length count in the CCW exceeds the key length on the record, the search operation ends when the key has been completely read. A successful comparison causes the next command to be skipped. If the length count in the CCW is less than the key length on the record, the comparison of the data coming from main storage with the data coming from the disk drive continues until the number of bytes specified in the CCW has been compared. If the search conditions of this short field are satisfied, the next command is skipped.

When a 'search key equal' command is issued for a record with a key length of zero, the result of the comparison is never equal. If a 'search key equal' command is issued for such a record and a 'read data' command follows in the chain, the data field to be read is that of the next record encountered.

If a bus out parity error is detected during the search operation, unit check, channel end and device end are generated.

A 'search key equal' command is executed whether or not it is preceded by another command.

Search Key High

The 'search key high' command has a similar effect to the 'search key equal' command except that the comparison determines whether the key received from the disk drive is higher than the key in main storage.

Search Key Equal or High

The 'search key equal or high' command has a similar effect to the 'search key equal' command except that the comparison determines whether the key received from the disk drive is equal to or higher than the key in main storage.

Sense Commands

Sense I/O

The 'sense I/O' command causes 24 bytes of sense information to be transferred from the disk attachment to main storage. The bytes identify the error or unusual condition which caused the last unit check. When the unit check bit is set in the CSW for a disk storage device, all other disk storage devices on the system will respond to further addressing with control unit busy.

After the sense information has been transferred to main storage, the next command in the chain is read out, or, if the chain has been completely executed, channel end and device end are presented.

Sense information is reset to zero whenever an initial status byte of zero is given in response to an instruction other than 'test I/O' or a command other than 'no-operation'.

Read Buffered Log

The 'read buffered log' command causes 24 bytes of usage and error statistics to be transferred from the disk attachment to main storage and to the SVP. The statistics refer to the device addressed by the 'start I/O' instruction and the drive identified by sense byte 4. The statistics are reinitialized after the data has been transferred.

If the byte count in the CCW is less than 24, only the specified number of bytes is transferred to main storage. If the byte count in the CCW is greater than 24, only 24 bytes are transferred to main storage.

Control Commands

Control commands do not cause a transfer of data between a disk drive and main storage. In certain control operations, however, a few bytes may be transferred between main storage and the disk attachment.

No-Operation

The 'no-operation' command causes no action at the disk drives. It is processed as an immediate command.

The 'no-operation' command should be used with care, otherwise results are unreliable. If a 'no-operation' is chained, a record may be partly or wholly skipped. For example, if a 'no-operation' command is given between 'read count' and 'read data' commands, the data area of one record is skipped, and the data area of the following record is read.

Seek

The 'seek' command causes the seek address to be transferred from main storage to the disk attachment. The attachment selects the disk drive, moves the access mechanism to the specified cylinder, and selects a read/write head.

Six address bytes are required. If the length count in the CCW exceeds six, only six bytes are transferred. If the count is less than six, or if the seek address is invalid, the command is rejected, and channel end, device end, and unit check are set in the CSW.

When the seek address has been transferred, the access mechanism is moved, if necessary. If no mechanical motion is required, however, and the command is last in the chain, device end is presented. If mechanical motion is required, and the command is last in the chain, channel end is set in the initial status and device end is set when the mechanical motion is complete.

Seek Cylinder

The 'seek cylinder' command has the same characteristics as the 'seek' command.

Seek Head

The 'seek head' command causes the seek address to be transferred from main storage to the disk attachment. The disk attachment selects the head on the specified disk drive. The cylinder address bytes are checked for validity and no access motion is initiated.

Six address bytes are required (Figure 66). If the length count is less than six, or if the seek address is invalid, the command is rejected, and channel end, device end, and unit check are set in the CSW. If the 'seek head' command is last in a chain, channel end and device end are presented when the seek address has been transferred.

Space Count

The 'space count' command is used to bypass a defective area of track in order to recover the following data. The command can have two different effects, depending on its position in a chain.

If the 'space count' command *is not chained* from a read, search, write or another 'space count' command, it causes the disk attachment to:

1. Search for index point.
2. Count over gap one, the home address, and gap two.
3. Space over the count area of record zero, while three bytes of data are fetched from storage.
4. Set an 'end of count area' internal indicator.
5. Read out the next command in the chain.

Thus, the 'space count' command can be used to recover or bypass a defective count area on record zero. When the 'space count' command is followed by a 'read key and data' command, the disk attachment reads the key and data areas of record zero. If the track contains only the home address, the disk attachment sets data check (sense byte 0, bit 4).

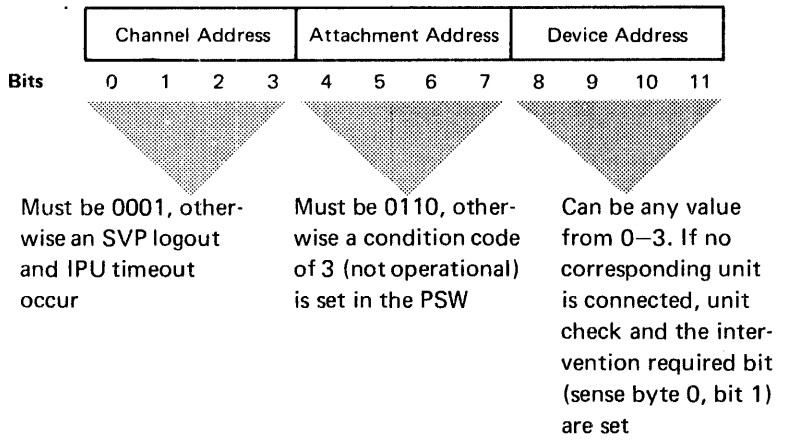
When the 'space count' command is followed by a 'read count, key and data' command, the disk attachment reads record one. If the track contains only the home address, or only the home address and record zero, the disk attachment sets the no record found bit (sense byte 1, bit 4).

If the 'space count' command *is chained* from a read, search, write or another 'space count' command, it causes the disk attachment to:

1. Find the beginning of the next count area (including that of record zero).
2. Space over the count area, while three bytes of data are fetched from main storage.

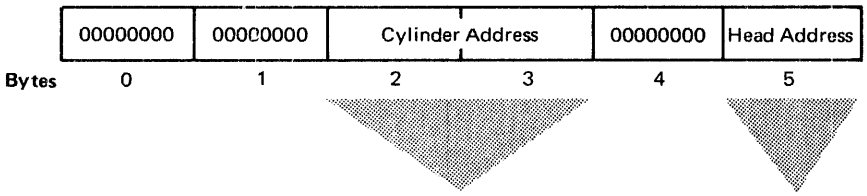
Device Addresses

This illustration shows the format of a 12-bit address used in addressing disk storage devices.



Seek Addresses

This illustration shows the format of the 6-byte seek address read out by a seek command to select a track on a disk drive within a 3340 facility. The seek command is rejected if the format is violated.



35-megabyte data module:

	0–349	*0–11*
Data tracks	0–347	0–11
Alternate track	348	0–11
CE track	349	0–11

70-megabyte data module:

	0–696	*0–11*
Data tracks	0–692	0–11
Alternate track	693–694	0–11
CE track	695–696	0–11

3340 Disk Addressing

Figure 66. 3340 Disk Addressing [10845]

3. Set an 'end of count' internal indicator.
4. Read out the next command in the chain.

Thus, the 'space count' command can be used to bypass a bad count area. As an example, if record N has a defective count area, the following sequence may be used to recover its key and data areas, provided record N is not record zero, and provided the key length and data length are known and are supplied by the 'space count' command:

Read home address
Search identifier (record N – 1)
TIC* – 8
Space count
Read key and data.

The first byte of data fetched from main storage by a 'space count' command is used as the key length, and the last two bytes are used as the data length. If the length count in the CCW exceeds three, only three bytes are transferred. If the count is less than three, the number of bytes specified in the CCW is transferred, and a value of zero is assumed for the remainder.

If the 'space count' command is chained from any formatting write or an 'erase' command, the command reject bit (sense byte 0, bit 0) is set. This bit is also set if a write, 'erase' or 'set file mask' command is issued in the same chain following the 'space count' command, or if the index point is detected before the 'space count' command has been completely executed.

Recalibrate

The 'recalibrate' command causes the disk drive to seek cylinder zero and head zero. A 'recalibrate' command is permitted by the same file protection mask as a seek command.

The 'recalibrate' command is not an immediate command: it normally presents an initial status byte of zero if it is the first command in a chain. Because there is no data transfer, the SLI bit must be set.

The disk attachment presents channel end in the ending status. If the 'recalibrate' command is last in the chain, device end is set in the CSW when the operation is completed.

Restore

The 'restore' command does not cause any operation in the disk attachment or the disk drives: it is provided for compatibility with other IBM direct access storage devices. If this command is first in a chain, the disk attachment presents an initial status of zero. If it is last in a chain, channel end and device end are set in the CSW when the final status is reported.

The 'restore' command is not an immediate command. Because there is no data transfer the SLI bit must be set.

Set File Mask

The 'set file mask' command causes one byte of data to be transferred from main storage to the disk attachment. This byte specifies which write and seek command can be executed. Bits 0 and 1 permit or inhibit write commands as shown in the following table:

Bit 0	*Bit 1*	*Meaning*
0	0	All write commands except 'write home address' and 'write record zero' are permitted.
0	1	All write commands are inhibited.
1	0	All write commands except formatting write commands are permitted.
1	1	All write commands are permitted.

Bits 3 and 4 permit or inhibit seek commands as shown in the following table:

Bit 3	*Bit 4*	*Meaning*
0	0	All seek commands are permitted.
0	1	Only the 'seek cylinder' and 'seek head' commands are permitted.
1	0	Only the 'seek head' command is permitted.
1	1	All seek commands and head switching are inhibited.

Bits 2 and 6 of the mask must be zero, otherwise the 'set file mask' command is rejected. Bit 5 must also be zero.

A 'set file mask' command can be located anywhere within a chain. When the command chain has been completely executed, all bits in the file mask are reset.

If a 'set file mask' command is issued more than once in a command chain, unit check is presented in the initial status and command reject (sense byte 0, bit 0) is set. If a write command is issued in violation of the file mask, unit check and command reject are set. If a seek command is issued in violation of the file mask, unit check and the file protected bit (sense byte 1, bit 5) are set. If a multi-track or overflow operation violates the seek portion of the file mask, unit check and the file protected bit are set.

A system reset causes the file mask to be set to zero, which means that the 'write home address' and 'write record zero' commands are inhibited.

Set Sector

The 'set sector' command causes one byte of information to be transferred to the disk attachment. The byte specifies a sector number. Each addressable track has 64 such sector numbers.

If the rotational position sensing feature *is not installed* in the disk attachment, the 'set sector command' causes no operation to be performed and track orientation is lost. Channel end and device end are set together in the final status.

If the rotational position sensing feature *is installed,* the disk attachment checks the validity of the byte transferred

by the 'set sector' command. If the argument exceeds 63 but is less than 255, the command is rejected, and unit check, channel end and device end are presented in the ending status.

The 'set sector' command is used when the disk attachment is working in block multiplexing mode. When the attachment receives a valid angular position argument, it disconnects the disk drive and is free for operations on another disk drive. When the specified sector number is reached, the disk attachment reconnects the disk drive and continues processing.

If the 'set sector' command is executed with an argument of 255, and is last in the chain, the disk attachment presents channel end and device end together in the final status; no operation is performed and track orientation is lost. If the 'set sector' command is executed with an argument of zero, the disk attachment attempts to reconnect just before the index point arrives at the read/write head.

Except for the value 255, all valid arguments transferred by the 'set sector' command are adjusted in the disk attachment to compensate for reselection delay.

The following formula is used to calculate the sector corresponding to a record (record n). The fractional portion of the calculated sector number should be ignored. A standard record zero area is assumed (KL=0, DL=8).

$$S(n) = \frac{1}{140}\left[353 + \sum_{i=1}^{n-1} (KL(i) + DL(i) + C)\right]$$

where C = 167 if KL(i) is zero,
C = 242 if KL(i) is not zero.

Note: The 'set sector' command does not guarantee record orientation; search commands must also be used.

Block Multiplexing

When the disk subsystem is operated in block multiplexing mode, up to four command chains (one for each attached disk drive) can be executed in the attachment at the same time. To enable block multiplexing, bit 0 of control register 0 must be set.

Block multiplexing permits data transfer to overlap with the mechanical motion of disk devices without causing an excessive number of CPU interruptions. It allows command sequences which involve long time-independent delays to be used without making the channel busy. The disk attachment stores the information necessary to control a temporarily "disconnected" command chain for each drive in the disk subsystem. A chain is disconnected if, after the issue of a seek or 'set sector' command, a delay occurs because the addressed drive is busy. The disk attachment is available during access motion and rotation delay.

If a unit check is detected during command chaining, the control unit is busy and the only disk drive available is the one addressed when the error occurred.

3340 TRACK AND RECORD FORMATS

Each addressable track begins at an index point and ends at the next index point. All tracks have the same basic format; home address, track description record, and one or more data records. Figure 67 shows the format of a 3340 disk track and its records. Figure 68 describes the sub-areas of a record.

Home Address

Each track has one nine-byte home address and six detection code bytes. The contents of the home address bytes define the physical location of the track.

The home address (and the standard record zero) is written at the IBM plant before the data module is sent to the user. If a skippable defect is found on the track, the appropriate entry is made in the skip displacement bytes. The control unit then skips the defect during subsequent operations.

Physical Address

The physical address is generated by the disk attachment, as defined in Figure 68.

Flag Byte

The flag byte bits provide the following information about defective recording areas.

Bit 0: When set, bit 0 indicates that the skip displacement bytes show a defect causing the count field of record zero to be displaced.

Bits 1 to 5: Bits 1 to 5 are not used, and are always zeros.

Bits 6 and 7: When set, bits 6 and 7 mark defective recording areas in the following way:

Bit 6	*Bit 7*	
0	0	Normal track
0	1	Alternate track
1	0	Defective track
1	1	Defective track

Cylinder Number and Head Number Bytes

The four-byte sub-area identifying the cylinder and head number (bytes 5 to 8) corresponds to the physical seek address of the track. The usual practice is for the operating system to copy this four-byte area from the home address into bytes 5 to 8 (cylinder and head) of the count area of each record during formatting.

Figure 67. 3340 Record Formats [10846]

Area	Sub-Area	Byte Length	Function
Count Area	Skip Displacement	2	Generated by disk storage control. In automatic surface defect handling, these bytes represent the displacement from the beginning of the G2 gap, which immediately follows the count area, up to the defect. If the count field is beyond the defect, or if automatic surface defect handling is not being used, the bytes are zero
	Physical Address	2	Generated by the disk attachment for seek verification. Byte 1, bits 0–7 Low order portion of the track cylinder address Byte 2, bit 0 Unused (zero) bit 1 High-cylinder address bit (binary 256) bit 2 Unused (zero) bits 4–7 Physical head address
	Flag Byte	1	Generated by the disk attachment. Bits 0, 1, 2 Automatic surface defect handling: Bit 0 Defect in next count field Bit 1 Defect in key field of this record Bit 2 Defect in data field of this record Bit 3 Unused (zero) Bit 4 Overflow record flag. Indicates that the logical record continues on next track. This bit is set in each segment of an overflow record except the last one Bit 5 Unused (zero) Bits 6–7 These bits mark defective recording areas, as follows: Bit 6 Bit 7 0 0 Normal track 0 1 Alternate track 1 0 Defective track 1 1 Defective track
	Identifier	5	Uniquely identifies a record regardless of its content. There are usually four track address bytes and one record number
	Key Area Length	1	Defines the length of the key area on the record. If the contents are zero, the key area and the following gap are omitted from the record
	Data Area Length	2	Defines the length of the data area. If the contents are zero it indicates the end-of-file record
	Detection Code Bytes	6	Used for error detection and correction when reading the count area
Key Area	Key	As defined in KL of count area, plus 6 detection code bytes	Identifies the information in the data area. Once formatting has been done, the contents of this area, but not its length, can be altered. If the key is changed, the data area must be re-written
	Detection Code Bytes	6	Used for error detection and correction when reading the key area
Data Area	Data	As defined by DL in count area, plus 6 detection code bytes	Stores the unit of user information defined by the key area. Once formatting has been done, the contents can be altered but not the length. A data area can be rewritten without affecting any other area in the record
	Correction Code Bytes	6	Used for error detection and correction when reading data area

Figure 68. 3340 Disk Record Sub-Areas [10847]

Record Zero

Record zero can be used as a normal data record but it is usually reserved for use by the operating system. Record zero differs from all other records in the following ways:

- Every addressable track contains only one record zero.
- Record zero is always the first record on a track after the home address.
- 'Read count', 'read count, key and data', and 'write count, key and data' commands do not operate on record zero. Special commands are available for reading and writing record zero only.
- The 'read key and data' command operates on record zero only if preceded in a command chain by a 'space count' command or by a search identifier command which has successfully searched for record zero.
- The 'read data' command operates on record zero only if preceded in a command chain by a 'space count' command, or by a search identifier or search key command which has successfully searched for record zero.
- Search key commands operate on record zero only if preceded in a command chain by a 'space count' command, or by a search identifier command which has successfully searched for record zero.
- The 'write data' command and the 'write key and data' command operate on record zero only if preceded by a search identifier command which has successfully searched for record zero.

Track Capacity

The number of records that can be written onto a track varies according to their length. The following equations, which also include the home address and the standard record zero (KL = 0, DL = 8), apply for the calculation of disk track loading:

$$\text{Track capacity} = 8{,}535 \text{ bytes}$$

$$\text{Bytes per record} = C + KL + DL$$

$$\text{Number of equal length records per track} = \frac{8{,}535}{C + KL + DL}$$

where C = 167 if key length (KL) is zero,
and C = 242 if key length (KL) is not zero.

The number of records (n) with different key and data lengths that can be written on a track must satisfy the following equation, in which a standard record zero has already been considered:

$$8{,}535 - \sum_{i=1}^{n} [C + KL(i) + DL(i)] \geq 0$$

where C = 167 if key length (KL) is zero,
and C = 242 if key length (KL) is not zero.

When record zero is not standard, the following formula should be used:

$$8706 > [KL(0) + DL(0) + C - 4 + \sum_{i=1}^{n} [KL(i) + DL(i) + C]$$

A table showing track loadings for equal size records of all possible lengths is available in the *Introduction to IBM 3340 Disk Storage,* GA26-1619.

3340 STATUS INFORMATION

The following paragraphs describe the meanings of the status indications given in response to 3340 commands.

Unit Status

The unit status information is recorded in CSW bits 32 to 39. The bits have the following meanings assigned:

Bit	*Designation*
32	Attention (not used)
33	Status modifier
34	Control unit end
35	Busy
36	Channel end
37	Device end
38	Unit check
39	Unit exception

Attention (Bit 32)

The attention bit is not used.

Status Modifier (Bit 33)

The status modifier bit is set when a search high, search equal, or search equal or high command has been executed and the search condition has been satisfied. If the status modifier bit is set together with the busy bit, the control unit is busy.

Control Unit End (Bit 34)

The control unit end bit is set when a previously presented control unit busy condition has been terminated. The bit is also set together with the unit check bit when a unit check condition is detected after device end has been set.

Busy (Bit 35)

The busy bit is set when the addressed 3340 is busy executing a previously-initiated command. The busy bit is also set if a command or an instruction (except 'test I/O') is issued to a 3340 for which status has not been cleared. If the busy bit is set together with the status modifier bit, the control unit is busy.

Channel End (Bit 36)

The channel end bit is set when the channel is available for further use. If command chaining is used, the channel end bit is set only for the last command in the chain.

Device End (Bit 37)

The device end bit is set when the 3340 is free to execute another command. The device end bit is set together with the channel end bit after the satisfactory completion of a command chain which did not require mechanical motion.

Unit Check (Bit 38)

The unit check bit is set when an error or unusual condition is detected in the disk subsystem. A system interruption occurs and information about the condition causing the unit check is available in the sense bytes, and can be retrieved by a 'sense I/O' command. For details of the conditions that can set unit check, see "3340 Sense Information" in this section.

Channel end and device end are always presented with unit check unless the unit check bit is set during initial selection.

Unit Exception (Bit 39)

The unit exception bit is set when an end-of-file record has been detected during execution of a 'read initial program load', 'read record zero', 'read count, key and data', 'read key and data', 'read data', 'write key and data', or 'write data' command. The unit exception bit is not set for 'read count', 'write count, key and data', or search key and search identifier commands. Unit exception status is generated when a data length of zero is detected in the count area of the end-of-file record. The key field, if any, is transferred when specified by the command.

Channel Status

The channel status is given in response to 3340 commands if these cause unusual conditions or were improperly specified. The channel status is indicated in bits 40 to 47 of the CSW, as follows:

Bit	*Designation*
40	Program-controlled interruption
41	Incorrect length
42	Program check
43	Protection check
44	Channel data check
45	Channel control check
46	Interface control check (not used)
47	Chaining check (not used)

The channel status bits (except the PCI bit) have the same standard functions for the 3340 as for any other device attached via a channel, integrated adapter or integrated attachment. These functions are described for the 2560 under "2560 Status Information" in the section "IBM 2560 Multi-Function Card Machine; Models A1 and A2". For a more detailed description of the channel status bits, see the *IBM System/370 Principles of Operation,* GA22-7000.

The following additional information on the PCI bit applies specifically to the 3340.

Program-Controlled Interruption (Bit 40)

The program-controlled interruption bit is set to indicate that the PCI flag bit was set in the CCW to which the status refers. The timing of the program-controlled interruption depends on the type of command given. For control commands, the interruption is signaled to the MIP when the control information has been transferred. For commands which are only given during orientation, the time when the interruption is requested depends on the amount of data to be handled.

If more than 256 bytes are to be transferred, the interruption is requested from the MIP during the data transfer. The interruption is dropped, however, if the MIP does not respond to the disk attachment during the transfer of the last 255 bytes. If the field is shorter than 256 bytes, the program-controlled interruption is not requested and the PCI bit is carried over to the new command.

3340 SENSE INFORMATION

There are 24 bytes of sense information available for the disk attachment and the 3340. The sense bytes are used for the following purposes:

- To identify the causes of the most recent unit check.
- To provide secondary information which the system may need for error recovery.
- To provide further information which may aid the customer engineer to diagnose a malfunction in the disk subsystem.
- To record usage information which indicates the number of bytes read and the number of times the access mechanism has moved to each logical address.

Sense information is made available to the program when a 'sense I/O' command is issued. The sense information also appears on the SVP log when a logout is made for a fault in the disk subsystem.

Sense bytes 0 to 2 are only generated when the unit check bit has been set in the CSW. These bytes provide general information on the error condition and indicate the action necessary for recovery. Sense bytes 0 to 2 also define the format of sense bytes 4 to 7 (which hold more detailed information about the error condition).

The following paragraphs describe the contents of the 24 sense bytes provided for the 3340.

Sense Byte 0

The bits in sense byte 0 have the following meanings assigned:

Bit	Designation
0	Command reject
1	Intervention required
2	(Not used)
3	Equipment check
4	Data check
5	Overrun
6	Track condition check
7	Seek check

Command Reject (Bit 0)

The command reject bit is set by any of the following conditions, which are defined more specifically in sense byte 7:

1. An invalid command, or a command associated with an uninstalled feature, is given.
2. Commands are given in an invalid sequence.
3. An invalid or incomplete argument is transferred as a result of a control command.
4. No home address is recorded on the track.
5. A write command is given which violates the file mask.
6. A write command is given when the write inhibit switch on the 3340 operator panel is in the READ position. The write inhibited bit (sense byte 1, bit 6) will also be set.
7. The flag byte transferred as a result of a 'write home address' command indicates that the home address area is to be moved down the track, but this flag byte does not show that the track is defective.

Intervention Required (Bit 1)

The intervention required bit is set when the addressed 3340 is not connected to the system or is not available for use, possibly because the motor is not running or a cover is open.

Equipment Check (Bit 3)

The equipment check bit is set when an unusual hardware condition has been detected in the disk attachment, the control unit or a disk drive. The conditions which set equipment check are defined in sense bytes 7 to 23.

Data Check (Bit 4)

The data check bit is set when a data error has been detected in the information transmitted from a 3340. If the correctable bit (sense byte 2, bit 1) is also set, the data error is correctable and sense bytes 15 to 21 provide the information which the system needs to correct the error. If the data error is uncorrectable, sense byte 7 identifies the condition specifically.

Overrun (Bit 5)

The overrun bit is set when a data byte is not received from the MSC in time to be written onto the data module, or was not received from the data module in time to be transferred to the MSC. When an overrun is detected, data transfer is stopped immediately.

If the overrun bit is set during a read operation, the data bytes from the disk drive are lost. In write operations, the lost portion of the record area is made up by valid zeros.

Track Condition Check (Bit 6)

The track condition check bit is set in any of the following situations.

1. Any single-track command other than 'search home address', 'read home address', or 'read record zero' is executed on a defective track.
2. The read/write mechanism switches to a defective track during execution of any multi-track or overflow command other than 'search home address', 'read home address', or 'read record zero'.
3. When, during any multi-track operation (including 'read home address', 'read record zero', or 'search home address'), or during any overflow operation, an attempt is made to continue processing from an alternate or defective track, whose status is known to the disk storage control. The storage control is aware of alternate or defective status only if some single-track read or search command has been executed on the track in the current command chain, and no control command other than no-operation has been executed since the single-track read or search command.

If a track condition interruption occurs, no read/write head switching is performed.

Seek Check (Bit 7)

The seek check bit is set when a disk drive has been unable to complete a seek operation because an equipment failure prevented the access mechanism from reaching the correct position.

Sense Byte 1

The bits in sense byte 1 have the following meanings assigned:

Bit	Designation
0	(Not used)
1	Invalid track format
2	End of cylinder
3	(Not used)
4	No record found
5	File protected
6	Write inhibited
7	Operation incomplete

Invalid Track Format (Bit 1)

The invalid track format bit is set when an attempt is made to write data in excess of track capacity. The bit is also set during a read or search operation when the index point is detected in the gap following a count field or key field.

Setting of the invalid track format bit indicates a programming error or the detection of an expected program condition.

End of Cylinder (Bit 2)

The end of cylinder bit is set when one of the following conditions occurs:

1. There is an attempt to continue beyond the addressable cylinder boundary during a multi-track read or search operation.
2. There is an attempt to continue beyond the addressable cylinder boundary during an overflow operation. The operation incomplete bit (sense byte 1, bit 7) is also set.

Setting of the end of cylinder bit indicates a programming error or the detection of an expected program condition.

No Record Found (Bit 4)

The no record found bit is set when the two index points have been detected during the execution of a command chain without an intervening read operation in the home address area or data area, or without an intervening write, 'sense I/O', or control command. Before the no record found bit is set, the disk attachment always verifies that the access mechanism is properly positioned.

Setting of the no record found bit indicates a programming error or the detection of an expected program condition.

File Protected (Bit 5)

The file protected bit is set when one of the following violations occurs:

1. A seek command has violated the file mask.
2. A multi-track read or multi-track search operation has violated the file mask.
3. An overflow operation has violated the seek portion of the file mask. The operation incomplete bit (sense byte 1, bit 7) is also set.

Setting of the file protected bit indicates a programming error or the detection of an expected program condition.

Write Inhibited (Bit 6)

The write inhibited bit is set when a write command has been issued to a disk drive which has its write protect switch on. The command reject bit (sense byte 0, bit 0) is also set.

Operation Incomplete (Bit 7)

The operation incomplete bit is set when one of the following conditions arises during the processing of an overflow segment:

1. The overflow violates a file-protected boundary. The file-protected bit (sense byte 1, bit 5) is also set.
2. The overflow violates a cylinder boundary. The end of cylinder bit (sense byte 1, bit 2) is also set.
3. A correctable data check is detected in a data field other than the last segment. The data check bit (sense byte 0, bit 4) and the correctable bit (sense byte 2, bit 1) are also set.
4. A defective or alternate track condition is detected after data transfer has begun. The track condition check bit (sense byte 0, bit 6) is also set.

Note: Sense byte 3 contains the restart command and sense bytes 7 to 23 provide information which further defines the error.

Sense Byte 2

The bits in sense byte 2 have the following meanings assigned:

Bit	*Designation*
0	RPS feature present
1	Correctable
2	(Not used)
3	Environmental data present
4	(Not used)
5	(Not used)
6	Data module size
7	Data module size

RPS Feature (Bit 0)

The Rotational Position Sensing (RPS) feature present bit is set when the RPS feature is installed in the selected drive.

Correctable (Bit 1)

The correctable bit is set when a data check (bit 4 set in sense byte 0) is correctable. Sense bytes 15 to 22 further identify the error.

Environmental Data Present (Bit 3)

The environmental data present bit is set to indicate that the sense data contains usage/error counter information. This bit is set in response to a 'read buffered log' command but *not* in response to a 'sense I/O' command.

Data Module Size (Bits 6 and 7)

The data module size bits define the capacity of the selected 3348 Data Module as follows:

Bit 6	*Bit 7*	*Meaning*
0	0	(Not used)
0	1	35 megabytes
1	0	70 megabytes
1	1	(Reserved)

Sense Byte 3

Sense byte 3 contains the restart command which is generated when the operation incomplete bit (sense byte 1, bit 7) is set. The restart command assists in identifying the operation which was in progress when the interruption, caused by the incomplete operation, occurred.

The restart command and the CSW provide information which can be used by the system recovery program to construct a new CCW, which is issued to the disk attachment to continue the operation at the point of interruption.

When the operation incomplete bit is set, the restart command is set to 06 (hexadecimal) if a basic read operation was in progress, or to 05 (hexadecimal) if a basic write operation was in progress. Sense byte 3 contains all zeros when the operation incomplete bit is off.

Sense Byte 4

Sense byte 4 identifies, in the following way, the physical drive and storage control that were addressed by a 'sense I/O' command.

Bit	*Identity*
0	Drive A
1	Drive B
2	Drive C
3	Drive D

Each of these physical drives may have been given any of the four 12-bit logical device addresses, so sense byte 4 allows the SVP to relate a disk module to its assigned address during logging. The sense information is thus identified with a physical drive.

Sense Byte 5

Sense byte 5 identifies the eight low-order bits of the cylinder address in the most recent seek argument, as follows:

Bit		
0	128	Cylinder number (low)
1	64	
2	32	
3	16	
4	8	
5	4	
6	2	
7	1	

Sense Byte 6

Sense byte 6 identifies the three high-order bits of the cylinder address and the four read/write head address bits in the most recent seek address, as follows:

Bit		
0	1024 Cylinder	Cylinder number (high)
1	512 Cylinder	
2	256 Cylinder	
3	0 (not used)	
4	8	Head
5	4	
6	2	
7	1	

Sense Byte 7

Sense byte 7 has two functions. Firstly, it specifies the format of sense bytes 8 to 23. Secondly, it provides message tables which give additional information on errors.

Figure 69 shows how bits 0 to 3 of sense byte 7 specify the format of sense bytes 8 to 23.

Bits *0 1 2 3*	Format of Sense Bytes 8 to 23
0 0 0 0	Format 0: Programming or system check
0 0 0 1	Format 1: Device and control unit equipment check
0 0 1 0	Format 2: Disk attachment equipment check
0 0 1 1	Format 3: (Not used)
0 1 0 0	Format 4: Data checks not providing displacement information
0 1 0 1	Format 5: Data checks providing displacement information
0 1 1 0	Format 6: Usage/error statistics

Figure 69. 3340 – How Sense Byte 7 Specifies Format of Sense Bytes 8 to 23 [10848]

For each of the formats shown in Figure 69 a unique message table is provided which defines the error condition more specifically. The error tables are formed by bits 4 to 7 of sense byte 7.

Sense Bytes 8 to 23

Sense bytes 8 to 23 define the various kinds of checks that can affect the 3340 disk subsystem. These bytes also provide usage/error statistics. The 16 bytes do not have unique assignments but their information content varies according to the format specified by bits 0 to 3 of sense byte 7. The seven formats available are listed in the description of "Sense Byte 7" in this section.

The error definitions given in sense bytes 8 to 23 may be of programming checks, system checks, equipment checks, or data checks, depending on the format. The usage/error statistics provide accumulated counts of significant events during subsystem operation, such as the number of bytes read and searched, and the number of access motions initiated by the channel.

The information provided by sense bytes 8 to 23 is mainly for the use of the customer engineer. For a full description see the *Introduction to IBM 3340 Disk Storage*, GA26-1619.

3340 ERROR RECOVERY

The following text describes the minimum action the operating system should take to deal with errors or unusual

conditions in the disk subsystem. Errors are usually indicated by the setting of unit check or any of the channel status bits except the PCI bit.

Unit Check in CSW

If unit check is set, the operating system should issue a 'sense I/O' command to retrieve the contents of at least sense bytes 0 to 2. The following paragraphs describe the suggested recovery procedures for conditions represented by these three bytes.

Command Reject (Sense Byte 0, Bit 0)

If the command reject bit is set, an invalid command or command sequence has been given, or the file mask has been violated. The operating system should provide a message for the operator, giving details of the erroneous command.

If the write inhibited bit (sense byte 1, bit 6) is set at the same time as command reject, a write command has been issued to a disk drive in the write inhibited state. A message to this effect should be transmitted to the operator.

Intervention Required (Sense Byte 0, Bit 1)

If the intervention required bit is set, the addressed disk drive is offline and the operating system should notify the operator by means of a message.

Equipment Check (Sense Byte 0, Bit 3)

The setting of the equipment check bit indicates an unusual condition in the hardware of the disk subsystem. The operating system should repeat the operation. If the error persists after ten retries, the operating system should retrieve sense bytes 7 to 23, analyze them, and place a message on the video screen for the operator.

Data Check (Sense Byte 0, Bit 4)

If the data check bit is set, a data error has been detected in the information transmitted from the disk drive. The operating system should examine the correctable bit (sense byte 2, bit 1) and, if it is set, perform the error correction function (ECF) as defined in *Introduction to IBM 3340 Disk Storage,* GA26-1619. If the correctable bit is not set, the operation should be retried and, if it is not successful after ten attempts, the operating system should notify the operator.

If a command chain has not been completely executed, the operating system should examine bit 3 of the next CCW (other than a transfer-in-channel command), and if this bit is set, revert to the user's command chain by issuing the following commands:

Command	*Remarks*
Seek	(The cylinder bytes and high-order head byte are obtained from the user's program. The low-order head byte is obtained from sense byte 6, bits 3 to 7.)
Set file mask	(Same as the original)
Set sector	(Sector in sense byte 13)
Search identifier equal	(Identifier in sense bytes 8 to 12)
TIC *-8	
TIC	(Command address in CSW)

If, however, bit 3 of the next CCW is zero, re-entry to the user's command chain is as follows:

Command	*Remarks*
Seek	(As described in preceding paragraph)
Set file mask	(Same as original)
Set sector	(Sector in sense byte 13)
Search identifier equal	(Identifier in sense bytes 8 to 12)
TIC *-8	
Read count	(Skip bit set)
TIC	(Command address in CSW)

If, in addition to the data check bit and the uncorrectable bit, the operation incomplete bit (sense byte 1, bit 7) is also set, re-entry into the user's command chain is as follows:

Command	*Remarks*
Seek	(With seek argument incremented by one)
Set file mask	(Same as original)
Set sector	(Argument 0)
Search identifier equal	(Record one)
TIC *-8	
Restart CCW 2	
TIC	(Command address in CSW)

Overrun (Sense Byte 0, Bit 5)

When the overrun bit is set, the operating system should retry the operation. If the overrun bit is still set after ten retries, a message should be transmitted to the operator.

Track Condition Check (Sense Byte 0, Bit 6)

If the track condition check bit has been set because of operations attempted *on a defective track,* the operating system should first retrieve the address of the alternate track from the identifier field of the record zero count area. After this new track address has been found by search operations, the original command chain can be resumed.

If the track condition check bit has been set because an operation continued *from an alternate track,* the operating system should update by one the seek argument of the defective track, using the track address in the identifier field of the record zero count area. The operation should then be resumed at this new address.

If the operation incomplete bit (sense byte 1, bit 7) is also set, the 3340 has switched *from* an alternate track, or *to* a defective track, during overflow record processing. In

the case of a defective track, the operating system should issue the following command chain:

Command	*Remarks*
Seek	(Address of alternate track)
Set file mask	(No seek command allowed)
Set sector	(Argument 0)
Search identifier equal	(Record 1)
TIC *-8	
Restart CCW 1	
TIC	(Command address in CSW)

In the case of an alternate track, the operating system should issue the following command chain:

Command	*Remarks*
Seek	(Address of defective track plus one)
Set file mask	(Same as original)
Set sector	(Argument 0)
Search identifier equal	(Record 1)
TIC *-8	
Restart CCW 1	
TIC	(Command address in CSW)

Seek Check (Sense Byte 0, Bit 7)

If the seek check bit has been set, a seek operation is incomplete or an incorrect physical address was read out from the home address or the count area. The operating system should issue a 'recalibrate' command, seek the original track address and repeat the operation. If the error persists after ten retries, the operating system should transmit a message to the operator.

Invalid Track Format (Sense Byte 1, Bit 1)

If the invalid track format bit is set, an attempt was made to write data in excess of track capacity. The operating system should transmit a message to this effect to the operator.

End of Cylinder (Sense Byte 1, Bit 2)

If the end-of-cylinder bit is set, a cylinder boundary has been detected during a multi-track operation. The operating system should increment the cylinder address in the current seek argument by one and reset the head address. Operation can be continued by executing the following command chain.

Command	*Remarks*
Seek	(Cylinder address plus one)
Set file mask	(Same as the original)
TIC	(Command address in CSW minus eight)

If the operation incomplete bit (sense byte 1, bit 7) is also set, a cylinder boundary has been detected during an overflow operation. The command chain can be continued by executing the following sequence of commands:

Command	*Remarks*
Seek	(Cylinder address plus one, head address reset)
Set file mask	(Same as original)
Set sector	(Argument 0)
Search identifier equal	(Record one)
TIC *-8	
Restart CCW 1	
TIC	(Command address in CSW)

No Record Found (Sense Byte 1, Bit 4)

When the no record found bit is set, the operating system should transmit a message to the operator to inform him that a programming error has been made.

File Protected (Sense Byte 1, Bit 5)

If the file protected bit is set, a seek command, a multi-track read, or multi-track search operation has violated the file mask.

In the case of a seek command, the operation can be continued by executing the following command chain:

Command	*Remarks*
Seek	(User's argument
Set file mask	(Same as the original)
TIC	(Command address in CSW)

In the case of a multi-track read or multi-track search operation, the following command chain should be used:

Command	*Remarks*
Seek	(Increment original seek argument by one)
Set file mask	(Same as original)
TIC	(Command address in CSW minus eight)

If the operation incomplete bit (byte 1, bit 7) is also set, the file violation occurred during an overflow operation, and re-entry to the command chain is as follows:

Command	*Remarks*
Seek	(Increment original seek argument by one)
Set file mask	(Same as original)
Set sector	(Argument zero)
Search identifier equal	(Record one)
Search identifier equal	(Record zero)
TIC *-8	
Restart CCW 1	
TIC	(Command address in CSW)

Environmental Data Present (Sense Byte 2, Bit 3)

If the environmental data present bit is set, statistical usage information is available and requires transfer to the SVP. The operation should be repeated once and, if the error persists, the operating system should transmit a message to the operator.

IBM 3410 Magnetic Tape Unit, Models 1, 2, and 3; IBM 3411 Magnetic Tape Unit and Control, Models 1, 2, and 3

This section describes the commands, status reports, and sense information for tape subsystems comprising 3410 Magnetic Tape Units, Models 1, 2 or 3; and a 3411 Magnetic Tape Unit and Control, Model 1, 2, or 3; operating under control of the magnetic tape adapter. Note that in any one subsystem, model numbers cannot be intermixed.

3410/3411 COMMANDS

Commands for the 3410s and 3411, which comprise the tape subsystem, are processed by the control unit, which is located within the 3411. For this reason, the enable/disable switch on the 3411 must be set to the ENABLE (on-line) position, otherwise the tape units will not respond to addressing by the program.

Note: The 3410 and 3411 are capable of command chaining but not of data chaining. If data chaining is specified, the command ends with program check (bit 42) set in the CSW.

Figure 70 shows the commands which are available for the 3410 and 3411.

Command Code									Command
Hex	*CCW Bits*								
	0	*1*	*2*	*3*	*4*	*5*	*6*	*7*	
01	0	0	0	0	0	0	0	1	Write
02	0	0	0	0	0	0	1	0	Read forward
0C	0	0	0	0	1	1	0	0	Read backward
07	0	0	0	0	0	1	1	1	Rewind
0F	0	0	0	0	1	1	1	1	Rewind-unload
17	0	0	0	1	0	1	1	1	Erase gap
1F	0	0	0	1	1	1	1	1	Write tape mark
27	0	0	1	0	0	1	1	1	Backspace block
2F	0	0	1	0	1	1	1	1	Backspace file
37	0	0	1	1	0	1	1	1	Forwardspace block
3F	0	0	1	1	1	1	1	1	Forwardspace file
C3	1	1	0	0	0	0	1	1	Set 1600 bpi-PE mode
CB	1	1	0	0	1	0	1	1	Set 800 bpi-NRZI mode
97	1	0	0	1	0	1	1	1	Data security erase
1B	0	0	0	1	1	0	1	1	Request track in error
4B	0	1	0	0	1	0	1	1	Set diagnose
03	0	0	0	0	0	0	1	1	Control no-op
04	0	0	0	0	0	1	0	0	Sense

Figure 70. 3410/3411 Commands [10849]

Write

The 'write' command causes data to be transferred from main storage to the selected tape unit where the data is written (recorded) on magnetic tape. The data transfer begins at the main storage location specified in CCW bits 8 to 31 and continues in ascending order of address (as the tape moves forward) until the length count in CCW bits 48 to 63 is reduced to zero. When the length count is reduced to zero, channel end and device end (bits 36 and 37 in the CSW) are both presented. If the operation runs into the end-of-tape area, channel end, device end, and unit exception (bit 39 in the CSW) are set and the TAPE INDICATE light is turned on at the tape unit.

A write operation may begin at the load point (a reflective marker attached to the tape at the beginning of the reel) or later, and previously-written information may be overwritten without error indication. The recording density and the recording method employed for a 'write' command depend on whether or not the Dual Density Tape Unit feature is installed.

If the dual density tape unit feature is installed, the density may be either 1600 bits per inch (bpi) phase-encoded (PE) or 800 bpi written using the non-return-to-zero inverted (NRZI) method, whichever was specified by a previously-given set mode command. The set mode command takes effect when the tape is positioned at the load point. The mode setting is retained as long as the tape is away from the load point and is reset when the tape returns to the load point. If no set mode command was given, the data is written at a density of 1600 bpi (PE). The parity is odd in each case.

If the dual density tape unit feature is not installed, data is written at a density of 1600 bpi, the parity is odd, and the recording method is phase-encoded.

The recording operation initiated by a 'write' command includes an automatic reading of each byte after it has been written. This automatic reading is performed by the second gap in the read/write head and is transparent to the program. If the parity of the byte is incorrect or the recorded amplitude is too low, an appropriate error indication is given.

When the tape is positioned at the load point and a 'write' command is given, the control unit provides format identification automatically, as follows:

1. If the density is specified at 1600 bpi, the phase-encoded identification burst is written first, then this burst is checked and an interblock gap is created. (Interblock gaps are created to separate blocks of written data.) Data recording then follows.
2. If the density is specified at 800 bpi, an erased area is created first, then data recording follows.

The presence or absence of the identification burst enables automatic density adjustment for subsequent read operations. When the write operation is completed, the tape stops after a nominal runout time which creates an interblock gap.

Read Forward

The 'read forward' command causes the magnetic tape at the selected tape unit to move forward; the recorded data is read and transferred to main storage. The data is stored into the main storage location specified in CCW bits 8 to 31. Data transfer continues in ascending order of main storage address until either the count in CCW bits 48 to 63 is reduced to zero or an interblock gap is found, whichever occurs first. The magnetic tape is, however, moved until the interblock gap is found regardless of how many bytes of data are transferred. This ensures that the read/write head is located in the interblock gap at command completion, ready for the next command. When the interblock gap is detected, channel end and device end are both presented. If a tape mark (a block of coded data) is detected during the read operation, unit exception is presented in addition to channel end and device end.

The format used for the read operation depends on whether or not the dual density tape unit feature is installed.

If the dual density tape unit feature is installed, the presence of the PE burst sets the reading density to 1600 bpi and the mode to PE. Absence of the PE burst sets the reading density to 800 bpi and the mode to NRZI. This occurs automatically so that no set mode command is required for read operations.

If the dual density tape unit feature is not installed, the density and mode for a read command can be only 1600 bpi, PE, as specified by the PE identification burst written behind the load point. The identification burst is checked for as the tape leaves the load point and applies until the tape returns to the load point. If the burst is not found, the read operation stops before the first data block, and unit check (bit 38 in the CSW) is set.

Read Backward

The 'read backward' command causes the tape at the selected tape unit to move backward; the recorded data is read and transferred to main storage starting at the main storage location specified in bits 8 to 31 of the CCW. Data transfer continues in *descending* order of address until either the count in CCW bits 48 to 63 is reduced to zero or the interblock gap is found, whichever occurs first. The tape moves until the interblock gap is found, regardless of how many bytes are transferred. When the gap is found, channel end and device end are both presented. If a tape mark is detected during the read operation, unit exception is presented in addition to channel end and device end. The density and mode in which the recorded data is read are determined as described for the 'read forward' command. If, during a read backward operation, the tape runs into the load point, the unit check bit in sense byte 0 is set.

Rewind

The 'rewind' command causes the selected tape unit to rewind the tape to the load point. Channel end is presented in the initial status, that is, as soon as the command is accepted. The tape unit then begins to rewind until the load point is detected. The drive stops, then moves the tape forward to the load point so that the unit is ready. Device end is then presented. If the tape unit has its tape already at the load point when the 'rewind' command is given, channel end and device end are both presented in the initial status.

Rewind Unload

The 'rewind unload' command causes the selected tape unit to rewind the tape to the load point, then to unload the tape so that it can be removed from the drive. Channel end, device end, and unit check are indicated in the initial status when the command is accepted. (The unit check status indicates that the tape unit is no longer ready.) The tape drive then rewinds the tape until the load point reflective marker is detected. The tape unit releases the vacuum upon detection of the load point, after which it is no longer in the ready state, and the tape can be removed.

Note: Subsequent installation of another tape, loading it, and pressing the START key causes device end status to be presented, indicating that the tape unit has been placed into the ready state.

Erase Gap

The 'erase gap' command causes the selected tape unit to move its tape forward and to erase information on the tape (if any). The results of this command depend on the mode to which the tape unit is set, and the position of the tape, at the time the command is given.

In PE mode, an 'erase gap' command given when the tape is at the load point causes writing of the PE identification burst, after which an erased area approximately 3.6 in. (91,44 mm) long is created. An 'erase gap' command given when the tape is away from the load point erases an area about 4.2 in. (106,7 mm) long. Successive 'erase gap' commands each add about 3.6 in. (91,44 mm) of erased area.

In NRZI mode, an 'erase gap' command given when the tape is at the load point erases an area about 6.5 in. (165,1 mm) long; no identification burst is written. An 'erase gap' command given when the tape is away from the load point erases an area about 4.2 in. (106,7 mm). Successive 'erase gap' commands each add another 3.6 in. (91,44 mm) of erased area.

For the 'erase gap' command, channel end and device end are both presented when the erase operation is completed at the tape unit. If the erase gap operation runs into the

end-of-tape (EOT) area, channel end and device end are accompanied by unit exception and control unit end (bit 34 in the CSW). The TAPE INDICATE light is turned on.

Write Tape Mark

The 'write tape mark' command causes the tape unit to move its tape forward and to write a tape mark. (A tape mark is a special block of bytes which defines the boundary of a file.) No data is transferred from main storage because the tape mark is generated by the tape control unit. Channel end and device end are both presented when the write operation is completed at the tape unit. Tape mark writing is checked by the control unit and up to 15 automatic retry attempts are executed if the tape mark cannot be written successfully.

The tape mark is not recognized as data. The tape marks written differ, depending on the mode in which the tape unit operates.

In PE mode, the tape mark consists of approximately 75 bytes, and is preceded by an interblock gap of about 0.6 in. (15,2 mm);

In NRZI mode, the tape mark consists of one byte followed by seven erased bytes followed by a longitudinal redundancy check (LRC) byte. The tape mark is preceded by a 0.6 in. (15,2 mm) interblock gap.

Note: If a write tape mark operation runs into the end-of-tape area, unit exception and control unit end accompany the channel end and device end status. The TAPE INDICATE light is turned on at the tape unit.

Backspace Block

The 'backspace block' command causes the tape at the selected tape unit to move backward until the next interblock gap or the load point is found, whichever comes first. This backward tape movement does not involve a data transfer to main storage. Channel end and device end are presented when the tape motion is completed. If a tape mark is encountered during the backspace operation, unit exception is always presented.

Backspace File

The 'backspace file' command causes the tape at the selected tape unit to move backward, either to the interblock gap located beyond the next tape mark or to the load point, whichever comes first. No data is transferred. Channel end and device end are both set when tape motion is completed.

Forwardspace Block

The 'forwardspace block' command moves the tape at the selected tape unit forward to the next interblock gap; no data is transferred. Channel end and device end are both set when tape motion is completed. If the forwardspace block operation runs into the end-of-tape area, the TAPE INDICATE light on the tape unit is turned on (no status indications other than channel end and device end). If a tape mark is detected during the forwardspace block operation, unit exception is presented in addition to channel end and device end.

Forwardspace File

The 'forwardspace file' command moves the tape at the selected tape unit forward to the interblock gap that follows the next tape mark. No data is transferred to main storage. Channel end and device end are both set when tape motion is completed. If the forwardspace file operation runs into the end-of-tape area, the TAPE INDICATE light is turned on but no status indication is given other than channel end and device end.

Set Mode Commands

The set mode commands can only be used if the dual density tape unit feature is installed. After initial power-on or system reset, all tape units are automatically set to write at 1600 bpi in phase-encoded mode. The set mode commands enable the density to be set to 800 bpi NRZI, or reset to 1600 bpi PE.

Notes:

1. Set mode commands apply only to the entire length of tape on a reel; it is impossible to change mode and density half-way through a reel.
2. Set mode commands do not affect read operations, which are self-adjusting.

The set mode commands are of the immediate type, and channel end and device end are both presented in the initial status when the command code has been transferred. If a set mode command is issued in the absence of the dual density feature, the command is equivalent to a 'control no-op'.

Set 800 BPI – NRZI Mode: When the 'set 800 bpi – NRZI mode' command is given, all tape units that have their tape positioned at the load point change to 800 bpi in NRZI mode for any subsequent write-type operations (such as 'write', 'erase gap', or 'write tape mark').

Those tape units which have their tape positioned away from the load point when the 'set 800 bpi – NRZI mode' command is given are not affected by the command. However, the command is stored in the 3411's control unit and takes effect as soon as a tape unit returns its tape to the load point. At this time, the drive resets to 1600 bpi but then changes to the mode stored in the control unit.

Set 1600 BPI – PE Mode: To reset from the 800 bpi – NRZI mode back to 1600 bpi PE, the 'set 1600 bpi–PE mode' command must be given. This command has an immediate effect on only those tape units with tape at the load point. Those with tape positioned away from the load

point will change to the new mode on return to the load point (unless another set mode command has been given before the tape has returned to the load point).

Data Security Erase

The 'data security erase' command causes the selected tape unit to move its tape forward and erase the information on the tape until the EOT reflective marker is found. Channel end is indicated when the command code is accepted, device end is indicated when the EOT marker is found.

The 'data security erase' command is executed only when it is chained to an immediately preceding 'erase gap' command. Under all other circumstances (such as when it is issued as a stand-alone or when chained to another command), it is rejected.

Note: The 'data security erase' command erases data only from the point at which the command is given until the EOT marker is reached. If the area beyond the EOT marker is to be erased, successive 'erase gap' commands must be used.

Request Track in Error

The 'request track in error' command causes sense byte 2 (the "track-in-error" byte) to be transferred from the main storage location specified in CCW bits 8 to 31 to the control unit. Sense byte 2 has been brought into main storage via the last 'sense' command given to the tape subsystem. Sense byte 2 shows which track has failed (if any). The control unit uses this byte as an aid to recovering the next data block that is read. Channel end and device end are both set when the transfer of sense byte 2 is completed.

Set Diagnose

The 'set diagnose' command is for use by IBM customer engineers only. Improper use of this command may cause loss of vital data on tape.

Sense Command

The 'sense' command causes sense information to be transferred from the 3411's control unit to the main storage location specified in CCW bits 8 to 31. The information is transferred in ascending order of this address until either all nine sense bytes have been transferred or the count in CCW bits 48 to 63 is reduced to zero, whichever occurs first. Then channel end and device end are both presented. For details of the contents of the sense bytes, see "3410/3411 Sense Information" in this section.

Control No-Op

The 'control no-op' command causes no action at the tape unit except that channel end, device end, and any other status conditions which may be present are stored at initial selection.

3410/3411 STATUS INFORMATION

The following paragraphs describe the status reports, and the circumstances under which the reports are given, for the 3411 and 3410s which comprise the tape subsystem.

Unit Status

The unit status is recorded in bits 32 to 39 of the CSW. The bits have the following meanings assigned:

Bit	*Designation*
32	Attention (not used)
33	Status modifier (not used)
34	Control unit end
35	Busy
36	Channel end
37	Device end
38	Unit check
39	Unit exception

Attention (Bit 32)

The attention bit is not used.

Status Modifier (Bit 33)

The status modifier bit is not used.

Control Unit End (Bit 34)

The control unit end bit is set when the tape subsystem has been addressed at a time when the control unit (in the 3411) was busy executing an operation. Control unit end is also set when the control unit detects an unusual condition after channel end has been presented in the initial status; this can occur only for 'rewind' or 'data security erase' commands. Control unit end is also presented for a 'halt I/O' or 'halt device' instruction.

Busy (Bit 35)

When the busy bit is set, the addressed tape unit is busy executing a previously-issued command such as 'rewind' or 'data security erase'. The busy bit is also set if the addressed tape unit has an interruption condition pending.

Channel End (Bit 36)

The channel end bit is set when the data transfer portion of a command is completed or, if only the command code is transferred, when the command code transfer is completed. The setting of channel end indicates that the channel is available for another command.

Device End (Bit 37)

The device end bit is set when an operation is completed at a tape unit. The setting of device end may coincide with channel end (with write, read, and read backward

operations etc) or may occur later (as with rewind and data security erase operations). Device end is set alone when a tape unit is manually put into the ready state, as when a new tape has been loaded and the tape unit's START key is subsequently pressed.

Unit Check (Bit 38)

The unit check bit is set for various errors or unusual conditions. If unit check is set, a subsequent 'sense' command shows the exact cause (for details, see "3410/3411 Sense Information"). Typical cases that cause the setting of unit check are backward commands that either run into the load point or are initiated when the tape is already at the load point. Unit check is also set when a 'rewind unload' command has been accepted, and indicates that the addressed tape unit is no longer ready.

Unit Exception (Bit 39)

The unit exception bit is set when a write-type command (such as 'write', 'write tape mark', or 'erase gap') runs into the EOT marker. This situation also turns on the tape unit's TAPE INDICATE light. The light is turned off by a backward command that again senses the EOT marker. Unit exception is also set when a 'read', 'read backward', 'forwardspace block' or 'backwardspace block' command detects a tape mark before the next interblock gap is found.

Channel Status

The channel status is recorded in CSW bits 40 to 47; the bits have the following meanings assigned:

Bit	*Designation*
40	Program controlled interruption
41	Incorrect length
42	Program check
43	Protection check
44	Channel data check
45	Channel control check
46	Interface control check
47	Chaining check

The channel status bits have the same standard functions for the 3410 and 3411 as for any other device attached via a channel, integrated adapter, or integrated attachment. These functions are described for the 2560 under "2560 Status Information" in the section "IBM 2560 Multi-Function Card Machine; Models A1 and A2". For a more detailed description of the channel status bits, see *IBM System/370 Principles of Operation,* GA22-7000.

3410/3411 SENSE INFORMATION

The 3411 and 3410 tape units comprising the tape subsystem provide up to nine bytes of sense information. The following paragraphs describe the information that can be obtained from the contents of the nine sense bytes.

Sense Byte 0

The bits in sense byte 0 have the following meanings assigned:

Bit	*Designation*
0	Command reject
1	Intervention required
2	Bus out check (not used)
3	Equipment check
4	Data check
5	Overrun
6	Word count zero (not used)
7	Data converter check (not used)

Note: Whenever any of the bits in sense byte 0 are set, unit check is set in the CSW.

Command Reject (Bit 0)

The command reject bit is set when an unassigned command is given, or a 'write', 'write tape mark', 'erase gap', or 'data security erase' command is given to a tape unit that is "file protected" (enable ring not installed). Command reject is also set in response to a 'data security erase' command that is *not chained* to a preceding 'erase gap' command.

Intervention Required (Bit 1)

The intervention required bit is set if the selected tape unit is not ready or non-existent.

Bus Out Check (Bit 2)

The bus out check bit is not used.

Equipment Check (Bit 3)

The equipment check bit is set in the following situations:
1. A tape mark cannot be written properly.
2. A tape unit momentarily loses its ready state.
3. An internal error occurs during tape motion.
4. The addressed tape unit does not accept a command.
5. A tape positioning or tachometer error occurs.
6. The tape velocity is incorrect.

Data Check (Bit 4)

The data check bit is set in the following situations:
1. "Noise" is detected during an NRZI read operation.
2. Uncorrectable parity errors occur.
3. Two or more tracks have an envelope or phase error.
4. Excessive skew is detected.
5. The end velocity of a read operation is incorrect.
6. The end of a record is detected too early or too late.
7. A signal is detected during a data security erase operation.

For a description of "envelope errors" and "skew", see the details of the corresponding bits under "Sense Byte 3".

Overrun (Bit 5)

The overrun bit is set when the main storage controller fails to send or accept data during data transfer (in which case the data transfer operation stops). The tape moves on to its normal stopping point.

Word Count Zero (Bit 6)

The word count zero bit is not used.

Data Converter Check (Bit 7)

The data converter check bit is not used.

Sense Byte 1

The bits in sense byte 1 have the following meanings assigned:

Bit	*Designation*
0	Noise
1	Tape unit status A
2	Tape unit status B
3	7-track TU (not used)
4	At load point
5	Write status
6	File protected
7	Not capable

Noise (Bit 0)

The noise bit is set when a data check occurs during PE operations. It is also set when data is detected during the last portion of a write delay during an NRZI write operation. Noise sets data check in sense byte 0 and, consequently, unit check in the CSW.

Tape Unit Status Bits

Tape unit status bits A and B together give the following information:

Status A	*Status B*	*Meaning*
0	0	Non-existent drive
0	1	Not ready
1	0	Ready and not busy
1	1	Ready and busy

Tape Status A (Bit 1): The tape unit status A bit is set when a tape unit has been selected and is ready.

Tape Status B (Bit 2): The tape unit status B bit is set when the selected tape unit is not ready (for example, START key not pressed) or could not be made ready because it was rewinding.

7-Track TU (Bit 3)

The 7-track TU bit is not used.

At Load Point (Bit 4)

The at load point bit is set whenever the selected tape unit is at the load point. The setting of this bit shows, for example, why a 'read backward' command cannot be executed. The at load point bit is reset to zero when the tape leaves the load point.

Write Status (Bit 5)

The write status bit is set when the selected tape unit is in write status, and is zero if the tape unit is in read status.

File Protected (Bit 6)

The file protected bit is set when the selected tape unit is ready but the "write enable" plastic ring is not mounted on the hub of the tape reel. File protected is also set when the tape unit is not ready.

Not Capable (Bit 7)

The not capable bit is set when the tape installation has no features installed (the tape units operate at 1600 bpi, PE only) and the PE-identification burst was not detected at the load point. The absence of the identification burst indicates that the tape on the selected tape unit is in NRZI mode, and thus cannot be used. Setting of the not capable bit sets unit check in the CSW.

Sense Byte 2

The bits in sense byte 2 contain information that is used only by the control unit itself, not the program. This is because the bits represent the track-in-error information. For PE read operations, each bit that is set represents a track that has a phase error or is dead. (A dead track is one that is damaged, or has never been written on.) For PE write operations, each bit that is set represents a track that has an envelope check (see "Sense Byte 3") or phase error.

During NRZI read operations, the bits in sense byte 2 represent the cyclic redundancy check (CRC) information. During NRZI write operations, sense byte 2 is not used and contains the code 03 (hex).

Sense byte 2 is made available to the tape control unit when the 'request track in error' command is given.

Sense Byte 3

The bits in sense byte 3 have the following meanings assigned:

Bit	*Designation*
0	Vertical redundancy check
1	Multiple track error (PE) or longitudinal redundancy (NRZI)
2	Skew
3	End data check (PE) or cyclic redundancy check (NRZI)
4	Envelope check (PE only)
5	1600 bpi
6	Backward
7	C-compare (not used)

Vertical Redundancy Check (Bit 0)

The vertical redundancy check (VRC) bit is set if a parity error which cannot be corrected occurs during a read or

read backward operation. The VRC bit is also set when the automatic read-back during write operations reveals a parity error. This sets data check in sense byte 0 and consequently unit check in the CSW.

Multiple Track Error (Bit 1)

The multiple track error bit is set only for PE operations if two or more tracks have an envelope dropout (recorded bits with poor amplitude) and/or a phase error in the same data block. Setting of the multiple track error bit sets data check in sense byte 0 and unit check in the CSW.

Longitudinal Redundancy Check (Bit 1)

The LRC bit is set for NRZI write operations if the LRC byte has bad parity, or in read operations if the LRC register does not contain all zeros. Setting of the LRC bit sets data check in sense byte 0 and unit check in the CSW.

Skew (Bit 2)

The skew bit is set when the data bits are not properly aligned during any read- or write-type operation. Setting of the skew bit causes data check in sense byte 0 and unit check in the CSW to be set but only when skew is detected during PE read or read backward operations or during NRZI write operations.

End Data Check (Bit 3)

The end data check bit is set only during PE read or write operations when a preamble and at least one data byte is sensed but the postamble is not found before the interblock gap is reached. (The preamble and postamble are 41-byte information fields that frame each data block.) Setting of the end data check bit sets data check in sense byte 0 and unit check in the CSW.

Cyclic Redundancy Check (Bit 3)

The cyclic redundancy check (CRC) bit is set only for NRZI operations if a CRC error is detected during read, read backward, or write operations (when the second gap reads back bad CRC parity). Setting of the CRC bit sets data check in sense byte 0 and unit check in the CSW.

Envelope Check (Bit 4)

The envelope check bit is set only for PE operations when the signal amplitude drops below an acceptable level during read, read backward, or write operations. It is also set when a phase error is detected. For write operations, setting of the envelope check bit always causes the setting of data check in sense byte 0 and unit check in the CSW. For read operations, data check and unit check are only set if the envelope check results in an uncorrectable error.

1600 BPI (Bit 5)

The 1600 bpi bit is set when the selected tape unit is set to 1600 bpi density. When the selected 3410 is in NRZI mode, the 1600 bpi bit is zero.

Backward (Bit 6)

The backward bit is set when the selected tape unit is in backward status. After a backward-type operation, the tape unit remains in backward status until a forward command (such as 'write') is given.

C-Compare (Bit 7)

The C-compare bit is not used.

Sense Byte 4

The bits in sense byte 4 have the following meanings assigned:

Bit	*Designation*
0	Tape unit positioning check
1	Tape unit reject
2	End of tape
3	(Not used)
4	(Not used)
5	Diagnostic track check
6	Tape unit check
7	Illegal command

Tape Unit Positioning Check (Bit 0)

The tape unit positioning check bit is set when an error causes a situation where the position of the tape cannot be determined and correction cannot be made successfully. This bit is set, for example, if a read operation goes beyond an interblock gap and forward or backward spacing fails to find an interblock gap. Setting of the tape unit positioning check bit sets the equipment check bit in sense byte 0 and, consequently, unit check in the CSW.

Tape Unit Reject (Bit 1)

The tape unit reject bit is set when a command cannot be set into the selected tape unit or the tape unit loses its ready state (even momentarily) during any tape motion operation except rewind or rewind unload. The setting of the tape unit reject bit sets equipment check in sense byte 0 and unit check in the CSW.

End of Tape (Bit 2)

The end of tape bit is set when the tape is located at or beyond the EOT marker. This bit is turned off only when the tape is moved backward past the reflective marker. If the end of tape situation occurs during a write, write tape mark, or erase gap operation, unit exception is set in the CSW.

Diagnostic Track Check (Bit 5)

The diagnostic track check bit is set if the error recovery procedure program issues a loop write-to-read diagnostic

command which detects a dead track or a phase error. Since this error may have been provoked by the diagnostic operation, unit check is not set in the CSW. The setting of the diagnostic track check bit thus acts as a warning (track in error indication is given).

Tape Unit Check (Bit 6)

The tape unit check bit is set when the selected tape unit has an internal error such as a lamp failure or vacuum failure in one of the vacuum columns. This bit is also set when a momentary loss of the ready state occurs during the execution of commands which cause tape motion (except 'rewind' or 'rewind unload'). The setting of the tape unit check bit also sets equipment check in sense byte 0 and unit check in the CSW.

Illegal Command (Bit 7)

The illegal command bit is set when an unassigned command has been issued to the tape subsystem. Setting of this bit sets command reject in sense byte 0 and unit check in the CSW.

Sense Byte 5

The bits in sense byte 5 have the following assignments:

Bit	*Designation*
0	New subsystem
1	New subsystem
2	Write tape mark check
3	PE identification burst
4	PE compare (not used)
5	Tachometer check
6	False end mark
7	Reserved for RPQ

New Subsystem (Bits 0 and 1)

The new subsystem bits together give the following meanings:

Bit 0	*Bit 1*	*Meaning*
0	1	A 3410/3411 magnetic tape subsystem is attached
0	0	A 3410/3411 magnetic tape subsystem is *not* attached
1	0	
1	1	

This information is needed because the sense information provided by the 3410 and 3411 is different from that provided by other magnetic tape units.

Write Tape Mark Check (Bit 2)

The write tape mark check bit is set when a tape mark cannot be written and read back without error. Up to 15 retry attempts are performed automatically and if these are unsuccessful, equipment check is set in sense byte 0 and unit check set in the CSW.

PE Identification Burst (Bit 3)

The PE identification burst bit is set when the identification burst cannot be written error-free. The setting of this bit causes unit check to be set in the CSW.

PE-Compare (Bit 4)

The PE-compare bit is not used.

Tachometer Check (Bit 5)

The tachometer check bit is set when the tape speed is too low or too high. The setting of this bit causes equipment check in sense byte 0 and unit check in the CSW to be set.

False End Mark (Bit 6)

The false end mark bit is set only for PE operations when the postamble is incorrect. Either the "all ones byte" (part of the postamble) is detected prematurely or, if the all ones byte is detected in time, too few zeros follow it. Setting of the false end mark bit sets data check in sense byte 0 and unit check in the CSW.

Reserved for RPQ (Bit 7)

The reserved for RPQ bit is set when a feature provided in response to an RPQ (request for price quotation) is installed.

Sense Byte 6

The bits in sense byte 6 have the following meanings assigned:

Bit	*Designation*
0	7-track unit (not used)
1	Short gap mode
2	Dual density
3	Alternate density
4 to 7	Tape unit model

7-Track Unit (Bit 0)

The 7-track unit bit is not used.

Short Gap Mode (Bit 1)

The short gap mode bit is set when the selected tape unit has adjusted to short gaps. This can occur only during read operations and acts as a warning; it does not indicate an error.

Dual Density (Bit 2)

The dual density bit is set when the selected tape unit is equipped with the dual density feature.

Alternate Density (Bit 3)

The alternate density bit is set when the selected tape unit is operating in 800 bpi – NRZI mode.

Tape Unit Model (Bits 4 to 7)

Bits 4 to 7 identify the magnetic tape unit models as follows:

Bit 4	*Bit 5*	*Bit 6*	*Bit 7*	*Meaning*
0	0	0	0	3410 and 3411 Model 1
0	0	0	1	3410 and 3411 Model 2
0	0	1	0	3410 and 3411 Model 3

Sense Byte 7

The bits in sense byte 7 have the following meanings assigned:

Bit	*Designation*
0	Lamp check
1	Left column check
2	Right column check
3	Ready reset
4	Data security erase
5	(Not used)
6	(Not used)
7	(Not used)

Lamp Check (Bit 0)

The lamp check bit is set when any of the photo-sensing light circuits (for example, load point, end of tape) are defective. A lamp check condition also sets the tape unit check bit in sense byte 4 and, consequently, sets unit check in the CSW.

Left Column Check (Bit 1)

The left column check bit is set when a loss of vacuum occurs in the left column of the tape unit after a tape has been loaded. This also sets the tape unit check bit in sense byte 4 and unit check in the CSW.

Right Column Check (Bit 2)

The right column check bit is set when a loss of vacuum occurs in the right column of the tape unit after a tape has been loaded. This also sets tape unit check in sense byte 4 and unit check in the CSW.

Ready Reset (Bit 3)

The ready reset bit is set when the RESET key is depressed after the START key has already been operated (the 3410 was in the start condition), or the ready state is lost for some other reason such as a malfunction.

Data Security Erase (Bit 4)

The data security erase bit is set when a data security erase operation is in progress. This bit is turned off when the EOT reflective marker is detected (operation is completed). The setting of the data security erase bit does not indicate an error.

Sense Byte 8

The bits in sense byte 8 have the following meanings assigned:

Bit	*Designation*
0	(Not used)
1	Feedthrough
2	(Not used)
3	End velocity check
4	No read-back data
5	Start velocity check
6	(Not used)
7	(Not used)

Feedthrough (Bit 1)

The feedthrough bit is set when the second gap of the read/write head senses data during the writing of the preamble. This is the correct mode of operation, and thus the feedthrough bit is not an error indication. (This bit is used as a diagnostic aid by IBM customer engineers.)

End Velocity Check (Bit 3)

The end velocity check bit is set when the tachometer velocity is incorrect at the end of a write operation. Setting of the end velocity check bit sets the data check bit in sense byte 0 and unit check in the CSW.

No Read-Back Data (Bit 4)

The no read-back data bit is set only for write operations when data is not read back (by the second gap in the read/write head) within a specified time. This situation also sets data check, hence unit check in the CSW.

Start Velocity Check (Bit 5)

The start velocity check bit is set when the tachometer velocity is still incorrect, at the start of a write operation, after successive retries have been performed. This sets the data check bit in sense byte 0 and unit check in the CSW.

IBM 5203 Printer Model 3

This section describes the commands, status reports, sense information, and error recovery procedures for the 5203 Printer Model 3, when operating under control of the integrated printer attachment.

5203 COMMANDS

Write Commands

Write commands cause data to be transferred from main storage to the print line buffer; the data transfer is followed by the execution of the electro-mechanical portion of the print operation, including carriage motion (if any). The data transfer begins at the storage location designated by the data address (bits 8 to 31 in the CCW) and proceeds in ascending order of address. The data transfer ends either when the print line buffer is filled or when the length count (bits 48 to 63 in the CCW) has been reduced to zero, whichever occurs first. The count should be 120 or 132 (decimal), depending on the print line width. If the output area contains more characters than appropriate for the print line width, or if the count is less than the print line width, incorrect length (bit 41 in the CSW) is indicated unless the SLI flag is set while the CD flag is off in the current CCW. Channel end (bit 36 is the CSW) is indicated when the data transfer from main storage to print line buffer is completed. Device end (bit 37 in the CSW) is indicated when the mechanical portion of the print operation (and carriage operation, if any) ends. Channel end and device end are interruption conditions (unless chaining is in progress).

The printer attachment accepts the write commands shown in Figure 71. The carriage specification for a write command applies to the left-hand (standard) carriage, unless the command is preceded by a 'prepare right-hand carriage' command, in which case the carriage specification applies to the right-hand carriage.

Command Code									Command
Hex	CCW Bits 0	1	2	3	4	5	6	7	
01	0	0	0	0	0	0	0	1	Write without spacing
09	0	0	0	0	1	0	0	1	Write and space 1 after printing
11	0	0	0	1	0	0	0	1	Write and space 2 after printing
19	0	0	0	1	1	0	0	1	Write and space 3 after printing
89	1	0	0	0	1	0	0	1	Write and skip to channel 1 after printing
91	1	0	0	1	0	0	0	1	Write and skip to channel 2 after printing
99	1	0	0	1	1	0	0	1	Write and skip to channel 3 after printing
A1	1	0	1	0	0	0	0	1	Write and skip to channel 4 after printing
A9	1	0	1	0	1	0	0	1	Write and skip to channel 5 after printing
B1	1	0	1	1	0	0	0	1	Write and skip to channel 6 after printing
B9	1	0	1	1	1	0	0	1	Write and skip to channel 7 after printing
C1	1	1	0	0	0	0	0	1	Write and skip to channel 8 after printing
C9	1	1	0	0	1	0	0	1	Write and skip to channel 9 after printing
D1	1	1	0	1	0	0	0	1	Write and skip to channel 10 after printing
D9	1	1	0	1	1	0	0	1	Write and skip to channel 11 after printing
E1	1	1	1	0	0	0	0	1	Write and skip to channel 12 after printing

Notes:

1. If a write and skip command specifies a channel for which no code exists in the buffer, the carriage does not move and the command ends with unit check set in the CSW and the no channel found bit 6 in sense byte 0.
2. If a write and skip command orders the carriage to go to the channel at which it is currently located, the form moves until that channel is detected the next time.

Figure 71. 5203 Write Commands [10850]

Carriage Control

The following paragraphs provide general information on carriage control, and more detailed information on those carriage control commands which cannot be classified as "immediate" or "delayed" commands; the carriage control buffer is also described. "Immediate Carriage Control Commands" and "Delayed Carriage Control Commands" are described later, under separate headings.

If the 5203 is equipped with a single feed (the single feed is standard), only one set of carriage control commands is available. This set consists of space and skip immediate commands. If the 5203 is equipped with the Dual Feed feature, two sets of carriage control commands are available. The first set consists of space and skip immediate commands identical to those available for a 5203 with single feed. The second set consists of space and skip delayed commands. The functional difference between immediate and delayed commands is described in the following text.

Space and Skip Immediate Commands: When the command code is transferred to the IOP, channel end is indicated at initial selection, after which the carriage operation is started. Device end is indicated when the mechanical operation in the 5203 is completed. For a 5203 with dual feed feature, whether the space or skip operation is executed on the left or right carriage depends on the preceding command. If the preceding command was a 'prepare right-hand carriage' command, the right carriage executes the operation; otherwise, the left carriage is used.

Space and Skip Delayed Commands: When the command code is transferred to the IOP, channel end and device end

are both indicated at initial selection and *no* mechanical operation is started. Instead, the space or skip specification is stored in the printer attachment. If the next command is one which addresses the left carriage, the stored information is used for the right carriage; this next command may be a space immediate, skip immediate, write and space, or write and skip, but no other command. When the command addressing the left carriage starts a mechanical operation on that carriage, the *delayed* command simultaneously starts the specified mechanical operation on the right carriage. Thus both carriages move simultaneously, the left one under control of the current command, the right under control of the previous (delayed) command. Device end is set for the current command when both carriages have completed their mechanical operation.

'Prepare Right-Hand Carriage' Command

The 'prepare right-hand carriage' command is available only if the 5203 is equipped with the dual feed feature, otherwise the command is rejected. The command code is:

Hex	*CCW Bits* 0	1	2	3	4	5	6	7
EB	1	1	1	0	1	0	1	1

The 'prepare right-hand carriage' command specifies that any following command which can be used for either feed – a "common" command – will apply to the right-hand carriage (or buffer). If a common command is not preceded by a 'prepare right-hand carriage' command, it applies to the left-hand carriage (or buffer). All write commands, space or skip immediately commands, and the 'load carriage control buffer' command are common commands.

When the 'prepare right-hand carriage' command is given, channel end and device end are presented at initial selection and the command becomes effective immediately. The command remains effective until after the next common, delayed, or 'reset right carriage controls' command is executed. Any subsequent common commands apply to the left feed unless a new 'prepare right-hand carriage' command is given. UCS, 'sense', and 'control no-op' commands do not reset the 'prepare right-hand carriage' command.

Note: Prepare and delayed commands both apply to the right-hand carriage. When a prepare command and a delayed command, or vice versa, are given in direct succession, the most recently-given command is effective and the preceding command is ignored. If, for example, a prepare command follows a delayed command, the next command given is subject to the prepare command; the delayed command is ignored. If a delayed command follows a prepare command, the next command given is subject to the delayed command; the prepare command is ignored. This rule allows the programmer to override previously given carriage-specifying commands at any time before giving a common command.

'Reset Right Carriage Controls' Command

The 'reset right carriage controls' command cancels any previously given 'prepare right-hand carriage' or delayed command that has not yet been executed. The 'reset right carriage controls' command does not cause any mechanical action. Channel end and device end are indicated at initial selection. The 'reset right carriage controls' command code is:

Hex	*CCW Bits* 0	1	2	3	4	5	6	7
07	0	0	0	0	0	1	1	1

The 'reset right carriage controls' command can be useful in error recovery, where pending prepare or delayed commands could cause undesired effects.

Carriage Control Buffer Structure

The carriage of a 5203 printer is not controlled by paper tape, but by a carriage control buffer. A standard 5203 has a single 112-byte buffer; a 5203 with the dual feed feature has two 112-byte buffers, one for each carriage.

Each carriage control buffer byte represents one line on the forms sheet so that byte 1 represents the first line of a sheet and byte 112 represents the last line of a sheet (assuming the largest possible sheet which is 14 inches from fold to fold). Each byte may be loaded with a number ranging from zero to 12 (corresponding to the channel numbers punched in the familiar carriage control paper tape, used on the IBM 1403 Printer and others). The zero represents no channel designation ("no punch"). The carriage control buffer byte codes are shown in Figure 72.

To designate the actual length of a form (specified for tape-controlled carriages by cutting the control tape to

	Buffer Byte Code Bits								**Meaning**
Hex	*0*	*1*	*2*	*3*	*4*	*5*	*6*	*7*	
00	0	0	0	0	0	0	0	0	No channel (no punch)
01	0	0	0	0	0	0	0	1	Channel 1
02	0	0	0	0	0	0	1	0	Channel 2
03	0	0	0	0	0	0	1	1	Channel 3
04	0	0	0	0	0	1	0	0	Channel 4
05	0	0	0	0	0	1	0	1	Channel 5
06	0	0	0	0	0	1	1	0	Channel 6
07	0	0	0	0	0	1	1	1	Channel 7
08	0	0	0	0	1	0	0	0	Channel 8
09	0	0	0	0	1	0	0	1	Channel 9
0A	0	0	0	0	1	0	1	0	Channel 10
0B	0	0	0	0	1	0	1	1	Channel 11
0C	0	0	0	0	1	1	0	0	Channel 12
0D..FF	0	0	0	1	0	0	0	0	End-of-sheet

Figure 72. 5203 – Carriage Control Buffer Byte Codes [10851]

size), an end-of-sheet specification can be set into any byte of the carriage control buffer. The end-of-sheet specification causes the counter (which monitors the position of the carriage) in the printer attachment to wrap around when end-of-sheet is recognized.

Assigning the End-of-Sheet Code: The end-of-sheet code must be set into the buffer byte that represents the last printable line of a given sheet. The last printable line of a sheet is determined by multiplying the sheet length (in inches) by the desired line spacing, which can be either six lines or eight lines per inch.

For example: a 12-inch sheet multiplied by eight lines per inch results in 96 printable lines per sheet. The end-of-sheet code must be assigned to line 96 (buffer byte 96). A 12-inch sheet used with six lines per inch spacing results in 72 printable lines per sheet, so the end-of-sheet code must be assigned to line 72. Correct end-of-sheet code assignment ensures that the carriage control buffer remains in synchronism with the form. If the end-of-sheet code is not assigned to the last printable line of a sheet, the control counter wraps around to zero too early (or too late) causing information for the next sheet to be printed on the last lines of the previous sheet. There is no error indication to show that the counter is not synchronized with the form.

'Load Carriage Control Buffer' Command

On a 5203 equipped with the dual feed feature, the 'load carriage control buffer' command applies to the right-hand buffer if preceded by a 'prepare right-hand carriage' command; otherwise it applies to the left-hand buffer. The command loads the applicable buffer with data from main storage; the carriage line counter is then reset to the first line (the carriage is assumed to be positioned to print the first line on the sheet).

Data is transferred from main storage to the carriage control buffer, starting at the main storage location specified in bits 8 to 31 of the CCW and proceeding in ascending order of address. The buffer is loaded in ascending order of position and this continues until the end-of-sheet code is detected, the buffer is filled, or the CCW count is reduced to zero, whichever occurs first.

If there is no end-of-sheet code, the buffer contents can be used for skip control but the line counter will wrap to zero when the largest allowable sheet (14 inches) plus 1 would wrap (this is the default value assumed in the absence of an end-of-sheet code). Consequently, in cases where the forms length is not 113, the operation is asynchronous (the counter is not synchronized with the forms). If a channel 1 code is absent, forms end is not recognized, the CARRIAGE RESTORE key has no function, and a forms check occurs. This is because the printer indicates "end of form" only when the FORMS switch has been operated and the channel 1 is detected thereafter. In the absence of a channel 1 code, the function of the CARRIAGE RESTORE key is suppressed to prevent the carriage runaway that would otherwise occur.

If the count in the 'load carriage control buffer' CCW is either greater than 112 or less than 112 (decimal), incorrect length is indicated unless the SLI flag bit is on and the CD flag bit is off in the CCW.

Channel end and device end are both presented when the load operation is completed.

Immediate Carriage Control Commands

Immediate carriage control commands apply to the left carriage unless preceded by the 'prepare right hand carriage' command, in which case they apply to the right carriage. For immediate carriage control commands, channel end is indicated when the command code is transferred, device end is given when the mechanical operation at the carriage is completed. Device end is an interruption condition (unless chaining is in progress).

If an immediate carriage control command is preceded by a 'prepare right-hand carriage' command, the "preparation" ends when the immediate carriage control command is executed or terminated. If the immediate carriage control command is rejected (not started) the preparation remains effective.

The immediate carriage control commands available for the 5203 are shown in Figure 73.

Command Code									Command
Hex	*CCW Bits*								
	0	*1*	*2*	*3*	*4*	*5*	*6*	*7*	
0B	0	0	0	0	1	0	1	1	Space 1 immediate
13	0	0	0	1	0	0	1	1	Space 2 immediate
1B	0	0	0	1	1	0	1	1	Space 3 immediate
8B	1	0	0	0	1	0	1	1	Skip immediate to channel 1
93	1	0	0	1	0	0	1	1	Skip immediate to channel 2
9B	1	0	0	1	1	0	1	1	Skip immediate to channel 3
A3	1	0	1	0	0	0	1	1	Skip immediate to channel 4
AB	1	0	1	0	1	0	1	1	Skip immediate to channel 5
B3	1	0	1	1	0	0	1	1	Skip immediate to channel 6
BB	1	0	1	1	1	0	1	1	Skip immediate to channel 7
C3	1	1	0	0	0	0	1	1	Skip immediate to channel 8
CB	1	1	0	0	1	0	1	1	Skip immediate to channel 9
D3	1	1	0	1	0	0	1	1	Skip immediate to channel 10
DB	1	1	0	1	1	0	1	1	Skip immediate to channel 11
E3	1	1	1	0	0	0	1	1	Skip immediate to channel 12

Notes

1. If a skip command specifies a channel for which no code exists in the carriage control buffer, the carriage does not move and the command ends with unit check set in the CSW and the no channel found bit (bit 6) set in sense byte 0.
2. If a skip command orders the carriage to go to the channel at which it is already located, and the preceding command was one that did move the carriage, then the form does not move and channel end and device end are presented. If the preceding command was a write without space, the carriage moves until that channel is detected the next time.

Figure 73. 5203 – Immediate Carriage Control Commands [10852]

Delayed Carriage Control Commands

Delayed carriage control commands apply to the right-hand carriage only and, therefore, need not be preceded by a 'prepare right-hand carriage' command. If a 'prepare right-hand carriage' command is given prior to a delayed command, the delayed information is stored and the preparation is terminated. Delayed commands are only valid for a 5203 with the dual feed feature. If a delayed command is given to a 5203 with single feed, the command is rejected.

Delayed commands cause channel end and device end to be indicated in the initial status. The mechanical operation at the right-hand carriage is performed when the next command (after the delayed command) is one that addresses the left carriage (for example, a space or skip immediate, write and space or write and skip command).

Figure 74 shows the delayed commands available for a 5203 with dual feed.

Command Code									Command
Hex	CCW Bits 0	1	2	3	4	5	6	7	
0F	0	0	0	0	1	1	1	1	Space 1 delayed
17	0	0	0	1	0	1	1	1	Space 2 delayed
1F	0	0	0	1	1	1	1	1	Space 3 delayed
8F	1	0	0	0	1	1	1	1	Skip delayed to channel 1
97	1	0	0	1	0	1	1	1	Skip delayed to channel 2
9F	1	0	0	1	1	1	1	1	Skip delayed to channel 3
A7	1	0	1	0	0	1	1	1	Skip delayed to channel 4
AF	1	0	1	0	1	1	1	1	Skip delayed to channel 5
B7	1	0	1	1	0	1	1	1	Skip delayed to channel 6
BF	1	0	1	1	1	1	1	1	Skip delayed to channel 7
C7	1	1	0	0	0	1	1	1	Skip delayed to channel 8
CF	1	1	0	0	1	1	1	1	Skip delayed to channel 9
D7	1	1	0	1	0	1	1	1	Skip delayed to channel 10
DF	1	1	0	1	1	1	1	1	Skip delayed to channel 11
E7	1	1	1	0	0	1	1	1	Skip delayed to channel 12

Notes:

1. If several delayed commands are issued before a left-carriage-affecting command could execute one of them, only the last delayed command given is executed with the next appropriate command. The other delayed commands are lost.
2. If a delayed skip command designates a channel for which no code is found in the buffer, the command ends with unit check set, the no channel found bit (bit 6) set in sense byte 0, and the right carriage does not move. If the delayed command designates a channel at which the carriage is already located, the carriage does not move if the delayed command is activated by a space/skip immediate command. The carriage does, however, move if the delayed command is activated by a write command.

Figure 74. 5203 – Delayed Carriage Control Commands [10853]

UCS Commands

Universal character set commands are always available because the UCS feature is a standard feature of the 5203. Figure 75 shows the UCS commands available for a 5203 with the UCS feature installed.

Command Code									Command
Hex	CCW Bits 0	1	2	3	4	5	6	7	
F3	1	1	1	1	0	0	1	1	Load UCS buffer with folding
FB	1	1	1	1	1	0	1	1	Load UCS without folding
73	0	1	1	1	0	0	1	1	Block data check
7B	0	1	1	1	1	0	1	1	Allow data check

Figure 75. 5203 UCS Commands [10854]

Load UCS Buffer with Folding

The 'load UCS buffer with folding' command causes data to be transferred from main storage to the UCS buffer. The data transferred represents the chain image. During transfer, the EBCDIC codes of the first, second, and third quadrants of the standard EBCDIC table are "folded" into the fourth quadrant of this table so that four different EBCDIC codes cause one and the same character to be printed. Because the quadrants of the EBCDIC table are identified by bits 0 and 1 of a byte, folding is technically accomplished by suppressing bits 0 and 1 during code comparison so that, effectively, the quadrant specification is ignored.

The data transfer begins at the main storage location specified in bits 8 to 31 of the CCW and proceeds in ascending order of address until the 240-byte UCS buffer is filled or the length count (bits 48 to 63 of the CCW) has been reduced to zero, whichever occurs first. At the end of the data transfer channel end and device end are both indicated. The UCS buffer remains loaded until it is reloaded or power goes off.

Load UCS Buffer without Folding

The 'load UCS buffer without folding' command is identical to the 'load UCS buffer with folding' command except that folding does not occur. Only one EBCDIC code corresponds to each print character.

Automatic UCS Buffer Initialization/Reloading

The UCS buffer is automatically initialized with a standard 48-character set at IMPL time, enabling the 5203 to operate even if no chain image is loaded. Any load UCS buffer command overwrites the initial value and the new pattern is at the same time recorded on the diskette. In the case of processor damage, the UCS buffer is automatically reloaded from the diskette so that the pattern last used is available.

Block Data Check

The 'block data check' command provides the means to suppress data checks that can occur if, for example, the print line buffer contains a character bit pattern that is not available in the UCS buffer.

The 'block data check' command is always available because UCS is a standard 5203 feature. The command causes neither data transfer nor any mechanical operation.

Only the command code is transferred, and channel end and device end are both set in the initial status. When 'block data check' is given, data checks are suppressed until either an 'allow data check' command is given or power goes off or a power-on reset occurs.
Note: The block data check command for the 5203 is not subjected to any restriction in use. It can be given at any time and can be included in a chain. Its blocking function is, however, effective only in UCS operations.

Allow Data Check

The 'allow data check' command resets the effect of a previously-issued 'block data check' command. The 'allow data check' command need only be given to reset a 'block data check' command; if neither command is given, data checks are allowed.

The 'allow data check' command causes neither data transfer nor any mechanical operation. Only the command code is transferred, and both channel end and device end are set in the initial status.
Note: The 'allow data check' command can be given at any time, and can be included in a command chain.

Control No-Op Command

The 'control no-op' command (command code 00000011) performs no function in the 5203. When this command is given, channel end, device end, and any other status conditions that exist at the time are indicated in the initial status.

Read Commands

No 'read' command is available for the 5203. A 'read' command issued to the printer is rejected.

Sense Command

The 'sense' command is usually given when unit check has been set in the CSW, and provides a means of transferring up to six bytes of sense information from the printer attachment to main storage. The sense bytes contain information about errors or unusual conditions in the 5203 or its controlling front end; the operating system analyzes this information before taking appropriate action to recover from the error(s). The 'sense' command code is:

Hex	*CCW Bits* 0 1 2 3 4 5 6 7
04	0 0 0 0 0 1 0 0

The sense information is stored into the main storage location specified by CCW bits 8 to 31, in ascending order of address. The number of sense bytes to be transferred is specified in CCW bits 48 to 63. Channel end and device end are both set when the transfer of sense information to main storage is completed.

For details of the information that can be obtained by use of the 'sense' command, see "5203 Sense Information" in this section.

5203 STATUS INFORMATION

The following text gives the meanings of the status indications which are given in response to 5203 commands.

Unit Status

The unit status is indicated in bits 32 to 39 of the CSW. The unit status is directly related to a command that has been given to, completed by, or terminated by the 5203. The bits are assigned the following meanings:

Bit	*Designation*
32	Attention (not used)
33	Status modifier (not used)
34	Control unit end (not used)
35	Busy
36	Channel end
37	Device end
38	Unit check
39	Unit exception

Attention (Bit 32)

The attention bit is not used.

Status Modifier (Bit 33)

The status modifier bit is not used.

Control Unit End (Bit 33)

The control unit end bit is not used.

Busy (Bit 35)

The busy bit, when set, indicates that the printer and its controlling front end logic are occupied with executing some previously-initiated operation. If busy is set together with channel end or device end, it indicates a pending status.

Channel End (Bit 36)

The channel end bit, when set, indicates that the data transfer part of a 5203 command, or the transfer of the command code, is completed.

Device End (Bit 37)

The device end bit, when set indicates that the 5203 has completed the mechanical portion of an operation (if any). Device end thus signals that the printer is free to accept and execute a new command. Device end is set alone when the printer is manually changed from the not-ready to the ready state (the printer's START key is pressed).

Unit Check (Bit 38)

The unit check bit is set for various errors or other unusual conditions that may have occurred in the 5203 and/or its controlling front end logic. Because the setting of unit check does not define the error condition, a 'sense' command should be issued to the 5203. The contents of the sense bytes will show the actual cause of unit check being set. For details of the conditions that can set unit check, see "5203 Sense Information" in this section.

The setting of unit check breaks command chaining.

Unit Exception (Bit 39)

The unit exception bit is set for a write and space or space immediate command if the "channel 12" code was detected during carriage motion. Unit exception is not indicated if channel 12 is detected during skipping. In case of a 5203 with dual feed, a 'sense' command will show which of the two carriages is involved (if not both).

Channel Status

The channel status information is recorded in bits 40 to 47 of the CSW; the bits have the following meanings assigned:

Bit	*Designation*
40	Program controlled interruption
41	Incorrect length
42	Program check
43	Protection check
44	Channel data check
45	Channel control check
46	Interface control check (not used)
47	Chaining check (not used)

The channel status bits have the same standard functions for the 5203 as for any other device attached via a channel, integrated adapter, or integrated attachment. These functions are described for the 2560 under "2560 Status Information" in the section "IBM 2560 Multi-Function Card Machine; Models A1 and A2". For a more detailed description of the channel status bits, see *IBM System/370 Principles of Operation,* GA22-7000.

Note: A set PCI flag bit in the first CCW after a 'start I/O' instruction is not recognized if the 'start I/O' instruction finds the 5203 is not available.

5203 SENSE INFORMATION

Sense Byte 0

The bits in sense byte 0 have the following meanings assigned:

Bit	*Designation*
0	Command reject
1	Intervention required
2	Bus out check
3	Equipment check
4	Data check
5	Chain buffer parity check
6	No channel found
7	Channel 9

Command Reject (Bit 0)

The command reject bit, when set, indicates that the current command was rejected either because it is not assigned to the 5203 or because the feature to which the command applies is not installed. The following situations cause command reject:

1. An unassigned command (such as a 'read') is issued to the 5203.
2. A delayed space or skip command is issued to a 5203 which does not have the dual feed feature installed.
3. A 'prepare right-hand carriage' command is issued to a 5203 which does not have the dual feed feature installed.

The fact that the current command has been rejected is indicated by the setting of unit check in the initial status. This unit check causes chaining (if specified) to be suppressed.

Intervention Required (Bit 1)

The intervention required bit, when set, indicates that operator intervention is necessary to continue because the 5203 has lost the ready state. The ready state is lost in the following situations:

1. The 5203's STOP key is pressed.
2. The train cartridge is not properly seated or has been removed.
3. The rear unit is open or the forms chute points upward (in the load position).
4. A forms jam has occurred (switching on the CHECK light).
5. The forms have run out (switching on the FORMS light).
6. A carriage sync check has occurred (switching on the CHECK light).
7. A chain sync check has occurred (switching on the CHECK light).
8. An overheat condition (thermal overload) occurred in the hammer unit or the 5203's electronics gate.
9. A hammer driver could not be reset, or the CE hammer-on check switch was accidentally operated, causing the coil protect bit (bit 2, sense byte 2) to be set.
10. The hammer bar right home position could not be detected or the shift clutch failed.

11. The check circuitry is defective, setting the any-hammer-on check bit, and also forcing the coil protect check bit, in sense byte 2.
12. An error occurred in the subscan counter, setting the subscan ring check bit in sense byte 2.
13. A chain buffer address register check has occurred, setting the bit of the same name in sense byte 2.

Setting of the intervention required bit causes unit check to be set in the CSW at the initiation of a 'start I/O' or 'test I/O' instruction or at device end time, depending on when the condition arises. Intervention required is reset when the printer is restored to the ready state.

Bus Out Check (Bit 2)

The bus out check bit is not used by the 5203.

Equipment Check (Bit 3)

The equipment check bit, when set, indicates that a program-correctable error occurred in the 5203 or the front end logic. The error is corrected the next time the 5203 is selected for a 'start I/O', 'halt I/O', or 'halt device' instruction.

The equipment check bit is set by one or more of the nine error conditions which are represented by the bits of sense bytes 4 and 5. For details of these conditions, see "Sense Byte 4" and "Sense Byte 5" in this section.

The detection of an equipment check causes unit check to be set at the time device end (with or without channel end) is set.

Note: Setting of the equipment check bit does not cause the 5203 to lose the ready state.

Data Check (Bit 4)

The data check bit can only be set when the 5203 has the UCS feature installed and data checks are not prevented by a 'block data check' command. Data check is then set when the print line buffer contains a character pattern for which no matching pattern is found in the UCS buffer during a UCS print operation. This is usually due to the wrong program being used.

The fact that data check is set is indicated by unit check being set in the CSW at device end time.

Chain Buffer Parity Check (Bit 5)

The chain buffer parity check bit is set to indicate a chain buffer parity error. A chain buffer parity check sets unit check at device end time.

No Channel Found (Bit 6)

The no channel found bit is set when a write and skip command, a write without space command that is executing a delayed skip command, or a skip immediate command did not find the channel code (in the carriage control buffer) to which the carriage was to advance. The setting of the no channel found bit causes unit check to be set at device end time.

Channel 9 (Bit 7)

The channel 9 bit, when set, indicates that a channel 9 code was detected in the carriage control buffer during the execution of a write and space, delayed space, or immediate space command. The same situation when caused by a manual space or any of the skip commands does not set the channel 9 bit. Setting of the channel 9 bit causes unit check to be set at device end time.

Sense Byte 1

Sense byte 1 contains carriage identification, which is required when the 5203 has the dual feed feature installed. The bits have the following meanings assigned:

Bit	*Designation*
0	(Not used)
1	(Not used)
2	(Not used)
3	(Not used)
4	Left carriage channel 12
5	Left carriage channel 9
6	Right carriage channel 12
7	Right carriage channel 9

Right Carriage Channel 9/12 (Bits 3 to 7)

Bits 3 to 7 are set only when the 5203 has the dual feed feature installed. The bits are used to interpret the meaning of unit exception (channel 12) or unit check (channel 9) when either one or both carriages are involved. The bits are independent so that the exact condition can be indicated for each carriage.

Sense Byte 2

The bits in sense byte 2 represent conditions which cause the 5203 to lose the ready state. The setting of one of these bits causes the intervention required bit to be set in sense byte 0. The bits in sense byte 2 have the following meanings assigned:

Bit	*Designation*
0	Common interlock
1	Forms check
2	Coil protect check
3	Subscan ring check
4	Chain buffer address register check
5	Hammer unit shaft check
6	Any-hammer-on check
7	Thermal overload

Common Interlock (Bit 0)

The common interlock bit is set to indicate that the 5203's rear unit is open, a train cartridge is removed or not properly seated, or the forms chute is in the load position.

Forms Check (Bit 1)

The forms check bit, when set, indicates that there is a paper jam in the forms tractors.

Coil Protect Check (Bit 2)

The coil protect check bit, when set, indicates that power was removed from the hammer circuits to prevent damage to the hammer coils.

Subscan Ring Check (Bit 3)

The subscan ring check bit is set if there is an error in the subscan ring counter or a drum emitter failure.

Chain Buffer Address Register Check (Bit 4)

This bit is set to indicate there is a loss of synchronism between chain buffer addressing and the actual position of the train at home pulse time.

Hammer Unit Shift Check (Bit 5)

The hammer unit shift check bit, when set, indicates a failure in a shift clutch, clutch photo emitter, or hammer bar right home switch.

Any-Hammer-On Check (Bit 6)

The any-hammer-on check bit is set to show that the hammer coils are no longer protected because of a failure in the coil protect monitoring circuits, or because the CE any-hammer-on test switch was operated. The bit is also set if the 'any-hammer-on' latch was not turned off because a hammer failed to fire.

Thermal Overload (Bit 7)

The thermal overload bit, when set, shows that hammer power was removed due to overheating in the hammer unit or the 5203's electronics gate.

Sense Byte 3

The bits in sense byte 3 have the following meanings assigned:

Bit	*Designation*
0 to 5	(Not used)
6	Left carriage sync check
7	Right carriage sync check

Carriage Sync Check (Bits 6 and 7)

The sync check bits, when set, indicate that the respective carriage did not move or did not perform the correct number of steps (possibly due to an emitter failure). A carriage sync check causes the 5203 to lose the ready state.

Sense Byte 4

The bits in sense byte 4 represent eight error conditions, any one of which can cause the equipment check bit to be set in sense byte 0. An equipment check caused by a condition in sense byte 4 is a program-correctable error. The bits have the following meanings assigned:

Bit	*Designation*
0	Hammer reset failure check
1	No fire check
2	Misfire check
3	Print data buffer parity check
4	Check bit buffer parity check
5	Chain buffer parity check
6	Buffer address register check
7	Clock check

Hammer Reset Failure Check (Bit 0)

This bit, when set, indicates that a hammer driver failed to reset when addressed for resetting.

No Fire Check (Bit 1)

The no fire check bit, when set, indicates that a hammer failed to fire when addressed for firing.

Misfire Check (Bit 2)

The misfire check bit is set to indicate that a hammer fired without being addressed.

Buffer Parity Checks (Bits 3, 4, and 5)

The buffer parity check bits for the print data buffer, check bit buffer, and chain buffer are each set to indicate a parity error in the buffer concerned.

Buffer Address Register Check (Bit 6)

This bit is set when an addressing error causes a subscan to seem excessively long.

Clock Check (Bit 7)

The clock check bit is set when extra clock steps (possibly due to "noise") are detected.

Sense Byte 5

Bit 0 in sense byte 5 represents one further error condition (in addition to those in sense byte 4) which, when set, causes the equipment check bit to be set in sense byte 0. This equipment check is a program-correctable error.

Bit	*Designation*
0	Open coil check
1	(Not used)
2	(Not used)
3	(Not used)
4	(Not used)
5	(Not used)
6	(Not used)
7	(Not used)

Open Coil Check (Bit 0)

The open coil check bit, when set, indicates that a hammer coil has burnt out.

5203 ERROR RECOVERY

The following paragraphs describe the minimum action the operating system should take when errors or other unusual conditions occur. Errors and other unusual conditions are usually indicated by the setting of unit check or any of the other status bits (except an end condition or busy) in the CSW.

Unit Check in CSW

When a command ends with unit check set in the CSW, the operating system should issue a 'sense' command and subsequently inspect at least sense byte 0 to find the reason for the unit check. The following text describes the suggested error recovery procedures for errors shown by the bits in sense byte 0.

Command Reject (Sense Byte 0, Bit 0)

The most likely cause of command reject being set is a programming error. Either a command not assigned to the 5203 has been issued, or the feature for which the command was intended is not installed. A typical error would be that 'prepare right-hand carriage' command or a delayed command was issued to a 5203 without dual feed feature.

The operating system should trace back the program and provide a message advising the system programmer to correct the error.

Intervention Required (Sense Byte 0, Bit 1)

If the intervention required bit is set, the printer has lost the ready state and manual intervention is required. The operating system should analyze sense byte 2 because this byte contains error information not shown by the 5203's indicator lights. An appropriate message should then be issued to the operator advising him of the error and requesting him to press the 5203's START key (to restore the ready state).

If the error is not obvious from the information in sense bytes 2 and 3, the message should advise the operator to check the indicator lights on the 5203's operator panel. These lights, as described below, can suggest the reason for the 5203 losing its ready state.

INTERLOCK Light On: The operator should make certain that the train cartridge is properly mounted, the rear unit is closed, and the forms chute is in the feed position (downward).

FORMS Light On: The operator should check whether new forms must be inserted. In the case of end-of-forms, the printer continues printing and the FORMS light is switched on when the channel 1 code is found in the buffer. The operator must then insert new forms and press the 5203's START key. (The end-of-forms feelers must be set into their cutouts, otherwise the FORMS light remains on.)

CHECK Light On: An error has occurred either in the 5203 or in the front end. Errors in the printer can be conditions such as a forms jam, a thermal overload (hammer unit or electronics gate), a chain sync check, any hammer on check, and so on.

If the CHECK light comes on, the operator should, as a first measure, press the printer START key (to reset the printer and make it ready). If the ready state cannot be obtained or if the error recurs, the CE must be called.

Equipment Check (Sense Byte 0, Bit 3)

If the equipment check bit is set, the operating system should analyze the data provided by sense bytes 4 and 5, and issue a message to the operator advising him of the condition. The program should then retry the last command or display the last print line on the video display. Equipment check conditions are not usually so severe that a retry would be ineffective. However, if equipment check persists, the CE should be notified.

Data Check (Sense Byte 0, Bit 4)

If the data check bit is set, the print pattern sent to the 5203 cannot be printed with the train cartridge currently fitted. In that case, the applicable train cartridge should be mounted and the matching type arrangement loaded into the UCS buffer, then the job should be repeated.

Chain Buffer Parity Check (Sense Byte 0, Bit 5)

If the chain buffer parity check bit is set, the operating system should repeat the operation. If the error persists, the CE should be notified. Reloading of the UCS buffer is not required because the hardware reloads the buffer automatically.

No Channel Found (Sense Byte 0, Bit 6)

If the no channel found bit is set, one of the carriage control buffers has been loaded with information that is not appropriate for the current program. The operating system should either reload the carriage control buffer or provide a message that indicates what type of control information is to be loaded. The operator may also be advised to check the forms on the printer to determine which control program is required.

Channel 9 (Sense Byte 0, Bit 7)

If Channel 9 is found, the operating system should take the appropriate action depending on the use and meaning of channel 9. The channel 9 indication may be a programming

error, such as the wrong carriage control information for the current program.

Unit Exception in CSW

If the unit exception bit is set in response to carriage motion commands, a channel 12 code was detected. Interpretation and subsequent action depends on the logical meaning assigned to channel 12. Unit exception in response to a 'load carriage control' buffer command requires program correction (that is, the missing end-of-sheet or channel 1 code must be inserted unless carriage control is not intended – such as in simple listing jobs where spacing only is used).

Channel Data Check in CSW

The channel data check bit is usually set as a result of a parity error in the data transferred (such as during a buffer load operation) between main storage and the printer attachment. The error is not severe because the parity has been corrected. The ouput at the printer is, however, unreliable and the operating system should either retry the operation or use the video screen to display the contents of the output area as it should have been printed. Retry should in any case be attempted. Repeated channel data checks require CE attention.

Note: If channel data check is set, the operating system should analyze storage location 176, which contains the limited channel logout. This logout shows how far the operation has progressed.

Channel Control Check in CSW

If the channel control check bit is set, the operation was terminated or may not have been started due to a severe error in the main storage controller or the bus system. The operation should be repeated and if the error persists, the CE must be called.

Note: If channel control check is found, the operating system should analyze storage location 176, which contains the limited channel logout. This logout shows how far the operation has progressed.

IBM 5425 Multi-Function Card Unit, Models A1 and A2

This section describes the commands, status reports, sense information, and error recovery procedures for the 5425 Multi-Function Card Unit, Models A1 and A2, when under control of the integrated card I/O attachment.

5425 COMMANDS

Figure 76 shows the commands which are available for the 5425.

Command Code									Command
Hex	*CCW Bits*								
	0	*1*	*2*	*3*	*4*	*5*	*6*	*7*	
04	0	0	0	0	0	1	0	0	Sense
02	0	0	0	0	0	0	1	0	Read and feed primary
82	1	0	0	0	0	0	1	0	Read and feed secondary
22	0	0	1	0	0	0	1	0	Read IPL mode and feed primary
A2	1	0	1	0	0	0	1	0	Read IPL mode and feed secondary
01	0	0	0	0	0	0	0	1	Write punch and feed primary
81	1	0	0	0	0	0	0	1	Write punch and feed secondary
05	0	0	0	0	0	1	0	1	Write punch primary
85	1	0	0	0	0	1	0	1	Write punch secondary
41	0	1	0	0	0	0	0	1	Write print and feed primary
C1	1	1	0	0	0	0	0	1	Write print and feed secondary
45	0	1	0	0	0	1	0	1	Write print primary
C5	1	1	0	0	0	1	0	1	Write print secondary
—	0	M	M	M	0	F	1	1	Control primary
—	1	M	M	M	0	F	1	1	Control secondary
0F	0	0	0	0	1	1	1	1	Set ERP mode
0B	0	0	0	0	1	0	1	1	Reset ERP mode

Notes:

1. The 'F' bit of a 'control primary' or 'control secondary' command represents card feeding. If it is set, the 5425 can perform a feed cycle.
2. The 'M' bits of a 'control primary' or 'control secondary' command represent a binary coded stacker number.

Bit Setting			*Meaning*
1	*2*	*3*	
0	0	0	: No-op if F=0, autoselect if F=1
0	0	1	: Stacker 1
0	1	0	: Stacker 2
0	1	1	: Stacker 3
1	0	0	: Stacker 4

All other codes are invalid.

Figure 76. 5425 Commands [10855]

Sense

The 'sense' command causes sense information to be transferred from the integrated card I/O attachment to main storage. A 'sense' command may be given at any time, but should always be given when unit check (bit 38) is set in the CSW. The sense bytes are transferred to main storage starting at the storage location specified in bits 8 to 31 of the CCW. Data transfer continues in ascending order of this address until either the maximum of eleven sense bytes are stored or the length count in CCW bits 48 to 63 is reduced to zero, whichever occurs first. Channel end and device end (bits 36 and 37 in the CSW) are presented together when the transfer is completed.

The error indicators in the sense bytes are reset by the next command other than a 'sense' or 'no-op', or the next instruction other than 'test I/O', 'halt I/O', or 'halt device', provided the 5425 is not busy. For a detailed description of the sense bytes and their contents, see "5425 Sense Information" in this section.

Read Commands

Read and Feed Primary

The 'read and feed primary' command causes a card in the primary wait station to be fed through the punch and print stations into a stacker; a new card from the primary hopper is fed through the read station into the vacated primary wait station. Punching, printing, and stacker selection of the card fed from the primary wait station depend upon preceding write and control commands.

The data on the card fed through the read station is read by column groups (1, 33, 65; 2, 34, 66; and so on) into a 96-byte read buffer. All 96 columns are read, checked, and translated from 8-bit 96-column card code to EBCDIC. After all 96 columns of data have been read into the read buffer, the data is transferred to main storage in ascending order of columns (1, 2, 3, 4, and so on). The data is stored in ascending order of address starting at the storage location specified in bits 8 to 31 of the CCW. Transfer continues until the count in CCW bits 48 to 63 is reduced to zero or 96 bytes have been transferred, whichever occurs first.

Channel end is set when data transfer from the read buffer to main storage is completed. Device end is set when the mechanical operation has reached an appropriate point in its cycle (see description of the device end bit under "Sense Byte 0" in "5425 Sense Information"). Channel end and device end are normally set separately for the 'read and feed primary' command.

Read and Feed Secondary

The 'read and feed secondary' command causes a card in the secondary wait station to be fed through the punch and print stations into a stacker, and a card from the secondary hopper to be fed through the read station into the vacated secondary wait station. Punching, printing and stacker selection of the card fed from the secondary wait station

depend on preceding write and control commands. The data on the card fed through the read station is read into the read buffer, transferred to main storage, and channel end and device end are set in the same way as for a 'read and feed primary' command.

Read IPL Mode and Feed Primary

The 'read IPL mode and feed primary' command causes the same action as the 'read and feed primary' command except that the data from the read station is converted into 96-column card read IPL mode format before being translated to EBCDIC and stored in the read buffer. The contents of a card read in read IPL mode are interpreted as follows for columns 1 through 64:

Normal Format		*Interpreted As*	
T1	D	T1	D
T2	D	T2	D
T3	D	T3	D
T1	C	T1	C
T2	C	T2	C
T3	C	T3	C
T1	B	T1	B
T1	A	T1	A
T1	8	T1	8
T1	4	T1	4
T1	2	T1	2
T1	1	T1	1
T2	B	T2	B
T2	A	T2	A
T2	8	T2	8
T2	4	T2	4
T2	2	T2	2
T2	1	T2	1
T3	B	–	–
T3	A	–	–
T3	8	T1	D
T3	4	T1	C
T3	2	T2	D
T3	1	T2	C

The table shows how the tier 3 bits (columns 65 through 96) are OR'ed with the normal C and D bits of columns 1 through 64 so that a six-bit System/3 card can be assembled to give an eight-bit code for the first 64 columns. If the CCW length count is greater than 64, any bytes in excess of 64 stored in main storage will be meaningless.

Read IPL Mode and Feed Secondary

The 'read IPL mode and feed secondary' command causes the same action as the 'read and feed secondary' command except that the data from the read station is converted into 96-column card read IPL mode format before it is translated to EBCDIC and stored in the read buffer.

Write Punch and Feed Primary

The 'write punch and feed primary' command causes data to be transferred from main storage to the 5425's 96-byte punch buffer and then initiates a feed cycle (if the data transfer was error-free). During the feed cycle a card in the primary wait station is fed through the punch station, where it is punched and checked, and then through the print station into a stacker. A card from the primary hopper is fed through the read station into the vacated primary wait station. Printing and stacker selection of the card fed from the wait station depend upon preceding write (print), and control commands.

The data transfer from main storage to the punch buffer starts at the main storage location specified in bits 8 to 31 of the CCW and continues in ascending order of address until the CCW count (bits 48 to 63) is reduced to zero or 96 bytes have been transferred, whichever occurs first. The data is stored in the punch buffer in EBCDIC. If the CCW count is less than 96, the remaining positions of the punch buffer will be automatically filled with blanks. Channel end is set when the punch buffer is full.

The data from the punch buffer is translated to 96-column card code while the card is being punched and checked by column groups (1, 33, 65; 2, 34, 66; and so on). After being punched, the card is moved from the punch station through the print station and into a stacker. Device end is indicated at an appropriate point in the punch eject cycle (see description of the device end bit under "Sense Byte 0" in "5425 Sense Information"). Channel end and device end are normally set separately for the 'write punch and feed primary' command.

The data from the card that is fed from the primary hopper through the read station is not read into the read buffer.

Write Punch and Feed Secondary

The 'write punch and feed secondary' command causes the same action as the 'write punch and feed primary' command except that a card from the secondary wait station is punched and a card from the secondary hopper is fed through the read station to the vacated secondary wait station.

Write Punch Primary

The 'write punch primary' command causes data to be transferred from main storage to the punch buffer in the same way as for a 'write punch and feed primary' command. No card motion takes place. Channel end and device end are set when the punch buffer is full.

Write Punch Secondary

The 'write punch secondary' command causes the same action as the 'write punch primary' command.

Note: When bit 0 of the CCW for a read, write or control command specifies the primary or secondary feed path, all

following read, write, and control commands must specify the same card path until a command is accepted that causes card motion.

Write Print and Feed Primary

The 'write print and feed primary' command causes data to be transferred from main storage to one of two 128-byte print buffers, and then initiates a feed cycle if the data transfer was error free. During the feed cycle, a card in the primary wait station is fed through the punch station and then into the print station where up to four 32-character lines are printed. The card is then stacked. Punching and stacker selection of this card during the feed cycle depend on preceding write punch, and control commands. A card from the primary hopper is fed through the read station into the vacated primary wait station.

The data transfer from main storage to a print buffer starts at the main storage location specified in bits 8 to 31 of the CCW and continues in ascending order of this address until the CCW count is reduced to zero or 128 bytes have been transferred, whichever occurs first. The data is stored in the print buffer in EBCDIC.

If the CCW count is less than or equal to 96, any remaining positions up to 96 in the print buffer are automatically filled with blanks and the 5425 prints the data on the card in three lines. If the count is greater than 96 but less than or equal to 128, any remaining positions up to 128 in print buffer are automatically filled with blanks and the 5425 prints the data on the card in four lines. Channel end is set when the print buffer is full.

The 128-byte print buffers are required because the data in a print buffer is printed one card feed cycle after the print buffer is filled. The print buffer is filled while the card is in the wait station. One card cycle feeds the card from the wait station through the punch station; a second card cycle feeds the card into the print station to be printed. A second write print and feed operation must be given during this second card cycle to maintain specified throughput. This means that print data for the second card must be transferred from main storage to a second print buffer before the data in the first buffer is printed on the first card.

Print buffer selection is controlled by the card I/O attachment and is transparent to the CCW. Device end is set at a point in the mechanical cycle when the punch buffer and at least one print buffer are free to be loaded from main storage.

The data from the card that is fed from the primary hopper through the read station is not read into the read buffer.

Write Print and Feed Secondary

The 'write print and feed secondary' command causes the same action as the 'write print and feed primary' command except that a card from the secondary wait station is printed and a card from the secondary hopper is fed through the read station to the vacated secondary wait station.

Write Print Primary

The 'write print primary' command causes data to be transferred from main storage to the print buffer in the same way as for a 'write print and feed primary' command. No card motion is initiated. Channel end and device end are set together when the print buffer is full.

Write Print Secondary

The 'write print secondary' command causes the same action as the 'write print primary' command.

Note: When bit 0 of the CCW for a read, write, or control command specifies the primary or secondary feed path, all following read, write, and control commands must specify the same card path until a command is accepted that causes card motion.

Control Commands

Control Primary

The 'control primary' command controls stacker selection and may initiate a feed cycle in the primary card path without data transfer to or from main storage. The normal destination for a card in the primary feed path is stacker 1 (autoselection) if no other stacker has been specified by a 'control primary' command. The stacker select specification of the 'control primary' command (bits 1, 2, and 3 of the CCW) applies to the card in the primary wait station. Once any command that initiates a primary feed cycle is accepted, the stacker specification for that feed cycle cannot be changed.

If bit 5 in the CCW of a 'control primary' command is off, the command causes no card motion and channel end is indicated in the initial status byte, followed by a device end indication. The command is then equivalent to a 'no-op'. If bit 5 is set, the command initiates a primary feed cycle. Channel end is set in the initial status and device end is indicated when the mechanical operation has reached an appropriate point in its cycle (see description of the device end bit under "Sense Byte 0" in "5425 Sense Information"). If a previous 'write punch primary' and/or 'write print primary' command was given, punching and/or printing will be performed during the feed cycle. The data from the card fed from the primary hopper through the read station is not read into the read buffer.

Control Secondary

The 'control secondary' command controls stacker selection and may initiate a feed cycle in the secondary

card path without data transfer to or from main storage. The normal destination for a card in the secondary feed path is stacker 4 (autoselection) if no other stacker has been specified by a 'control secondary' command. The stacker select specification of the 'control secondary' command (bits 1, 2, and 3 of the CCW) applies to the card in the secondary wait station. Once any command that initiates a secondary feed cycle is accepted, the stacker specification for that feed cycle cannot be changed.

If bit 5 of the CCW for a 'control secondary' command is zero, the command is invalid and, therefore, rejected. If bit 5 is set, the command initiates a secondary feed cycle. Channel end is set in the initial status and device end is set when the mechanical operation has reached an appropriate point in its cycle (see description of the device end bit under "Sense Byte 0" in "5425 Sense Information"). If a previous 'write punch secondary' and/or 'write print secondary' command was given, punching and/or printing will be performed during the feed cycle. The data from the card fed from the secondary hopper through the read station is not read into the read buffer.

Set ERP Mode

The 'set ERP (error recovery procedures) mode' command sets an ERP flag bit in the card I/O attachment. This flag conditions the attachment to operate in ERP mode. In ERP mode, normal write commands enable the 5425 to punch and print data that remains in the punch and print buffers as a result of previous write commands. The ERP flag, when set, prevents the buffers from being filled with new data by normal write commands.

Once ERP mode is set, it can be reset only by issuing a 'reset ERP' command or by a system reset operation. Pressing the NPRO key does not reset ERP mode. Any pending commands which have not yet been executed by a feed cycle are cancelled when the 'set ERP mode' command is issued. Cancelled commands are deleted from the command history table, and must be re-issued.

The 'set ERP mode' command causes no card motion. Channel end is indicated in the initial status, with device end following.

Application Note: Because write and print commands do not transfer data in ERP mode, these commands cannot be used for data chaining when ERP mode is on. If this is attempted, errors will occur because the length count is not reduced.

Reset ERP Mode

The 'reset ERP mode' command resets the ERP flag, allowing normal execution of subsequent write commands. The 'reset ERP mode' command causes no card motion. Channel end is indicated in the initial status, with device end following.

5425 STATUS INFORMATION

The following paragraphs describe the meanings of the status indications given in response to 5425 commands.

Unit Status

The unit status is recorded in bits 32 through 39 of the CSW. The unit status is directly related to a command that is either issued to or has been completed or terminated by the 5425. The bits have the following meanings assigned:

Bit	*Designation*
32	Attention (not used)
33	Status modifier (not used)
34	Control unit end (not used)
35	Busy
36	Channel end
37	Device end
38	Unit check
39	Unit exception (not used)

Attention (Bit 32)

The attention bit is not used.

Status Modifier (Bit 33)

The status modifier bit is not used.

Control Unit End (Bit 34)

The control unit end bit is not used.

Busy (Bit 35)

The busy bit is only set in the initial status and, when set, indicates that the 5425 is either busy executing a previously-given command or has outstanding status pending. The 5425 is busy from the time it accepts a command until device end status is presented for that command.

Channel End (Bit 36)

The channel end bit, when set, indicates that data transfer is complete or that no data transfer will occur. For 'sense', read, or write commands, the 5425 presents channel end status after data transfer to or from main storage. This means that received data is available in the input area of main storage or that the output area of main storage can be loaded with new data. For control commands, channel end is presented in the initial status.

Device End (Bit 37)

The device end bit, when set, indicates that the 5425 either has completed a current operation or has made a transition from the not-ready to the ready state. Device end indicates that the 5425 is available to accept a new command.

For commands causing a mechanical operation, the 5425 presents device end at an appropriate point in its

mechanical cycle. This point depends upon the mechanical operation performed but always occurs after the 5425 is finished with the buffer(s) used for that operation. For multi-function operations, device end is set after the read, punch, and print buffers are free, whichever occurs last. Device end is always set at least 20 ms before any feed decision point. For commands that do not cause a mechanical operation, device end is set with or immediately after channel end.

The 5425 sets device end whenever it has made a transition from the not-ready to the ready state. This will occur whenever either the primary or secondary card feed paths are made ready by the operator.

Unit Check (Bit 38)

The unit check bit is set for several errors or other unusual conditions that can occur in the 5425 or its controlling front end logic. When unit check is set, it indicates that the 5425 requires program and/or operator intervention. The exact cause of the setting of unit check is indicated by the contents of the sense bytes, which can be retrieved and transferred to main storage by a 'sense' command. For details of the conditions which can set unit check, see "5425 Sense Information". Unit check is presented with either the initial status, channel end or device end.

Unit Exception (Bit 39)

The unit exception bit is not used.

Note: For other card I/O devices, the unit exception bit acts as a last card indicator. For the 5425, end of file must be indicated by a card punched with a slash and an asterisk.

Channel Status

The channel status is given in conjunction with 5425 commands if the commands cause unusual conditions or are specified improperly. The channel status is indicated in bits 40 to 47 of the CSW; the bits have the following assignments:

Bit	*Designation*
40	Program-controlled interruption
41	Incorrect length
42	Program check
43	Protection check
44	Channel data check
45	Channel control check
46	Interface control check
47	Chaining check (not used)

The channel status bits have the same standard functions for the 5425 as for any other device attached via a channel, integrated adapter, or integrated attachment. These functions are described for the 2560 under "2560 Status Information" in the section "IBM 2560 Multi-Function Card Machine; Models A1 and A2". For a more detailed description of the channel status bits, see *IBM System/370 Principles of Operation,* GA22-7000.

5425 SENSE INFORMATION

The following paragraphs describe the contents of the eleven bytes of sense information provided for the 5425.

Sense Byte 0

The bits in sense byte 0 have the following meanings assigned:

Bit	*Designation*
0	Command reject
1	Intervention required
2	Bus-out check
3	Equipment check
4	Data check
5	Overrun (not used)
6	No card available
7	(Not used)

Note: Except for intervention required, the sense indicators in byte 0 are reset by the next command or instruction accepted by the 5425 other than a 'sense', 'no-op', 'halt I/O', 'halt device' or 'test I/O'.

Command Reject (Bit 0)

The command reject bit is set when either an unassigned command or an invalid command sequence is given to the 5425. An invalid command sequence is a sequence of intermixed primary and secondary commands. When bit 0 of the CCW for a read, write or control command specifies the primary or secondary feed path, all following read, write and control commands must specify the same card path until a command is accepted that causes card motion. Command reject is also set when a control command for the *secondary* card path has bit 5 of the CCW set at zero, that is, when the command is in effect a 'no-op'. The 'set ERP mode' and 'reset ERP mode' commands apply to both card paths and cannot cause a command reject. The setting of command reject causes unit check to be set in the initial status.

Intervention Required (Bit 1)

The intervention required bit, when set, indicates that operator intervention is required at the 5425 because of one of the following conditions:

1. The selected feed path (primary or secondary) is not ready for a command that initiates card motion for that path.
2. The 5425's STOP key has been pressed.
3. The 5425's cover is open.
4. A stacker is full.
5. The chip box is full or has been removed.
6. A hopper check has occurred (see "Sense Byte 1", Hopper Check).
7. A feed check has occurred (see "Sense Byte 1").
8. An emitter check has occurred.

The setting of intervention required causes unit check to be set in the initial status or at device end time.

Bus Out Check (Bit 2)

The bus out check bit is not used.

Equipment Check (Bit 3)

The equipment check bit, when set, indicates one of the following error conditions (none of which are considered severe):

1. Read check during an optical read operation.
2. Punch check during a mechanical punch operation.
3. Print data check during a mechanical print operation.
4. Print clutch check during a mechanical print operation.

For a more detailed description of these conditions, see "Sense Byte 1".

The operation during which equipment check is set continues to its normal ending point. Equipment check causes unit check to be set at channel end time for a read check, and at device end time for a punch check, print data check, or clutch check.

Data Check (Bit 4)

The data check bit is not used.

Overrun (Bit 5)

The overrun bit is not used. The 5425 is fully buffered and cannot overrun.

No Card Available (Bit 6)

The no card available bit, when set, indicates that a write punch, write punch and feed, write print, or write print and feed command was issued to a card feed path whose wait station is empty. The setting of no card available causes unit check to be set in the initial status.

Sense Byte 1

The bits in sense byte 1 act as check condition indicators which are used for error recovery procedures. Some of the bits in sense byte 1 are also summary indicators of more detailed conditions represented by the bits in sense bytes 3, 4, and 5. The bits in sense byte 1 have the following meanings assigned:

Bit	*Designation*
0	Read check
1	Punch check
2	(Not used)
3	Print data check
4	Print clutch check
5	Hopper check
6	Feed check
7	(Not used)

Read Check (Bit 0)

The read check bit is set if, during a read operation, an optical read comparison shows an unequal result at the end of read sample time. The setting of read check causes equipment check to be set in sense byte 0 and unit check is presented at channel end time. The conditions which can set read check are described in "Sense Byte 4" and "Sense Byte 5".

Punch Check (Bit 1)

The punch check bit is set if the punch unit checking data (derived from the piezoelectric crystal punch checking system) does not match the data in the punch buffer at punch check sample time. The setting of punch check causes equipment check to be set in sense byte 0 and unit check is presented at device end time. The conditions which can set punch check are described in "Sense Byte 4" and "Sense Byte 5".

Print Data Check (Bit 3)

The print data check bit is set when the print wheels lose synchronization with the card I/O attachment's print character counter. The setting of print data check causes equipment check to be set in sense byte 0. Unit check is presented at device end time.

Print Clutch Check (Bit 4)

The print clutch check bit is set when a print stepper clutch malfunction is detected, and indicates an error in positioning the lines of print on the card. The setting of print clutch check sets equipment check in sense byte 0. Unit check is presented in the initial status or at device end time.

Hopper Check (Bit 5)

The hopper check bit is set when a card has failed to feed out of the hopper. The setting of hopper check causes the setting of intervention required in sense byte 0 and the presentation of unit check at device end time.

Feed Check (Bit 6)

The feed check bit is set when one or more cards are mispositioned. The setting of feed check sets intervention required in sense byte 0 and unit check is presented in the initial status or at device end time. Feed check is a summary indicator for the conditions represented in sense byte 3.

Sense Byte 2

Sense byte 2 contains information about the location of cards in the 5425 transport at the time the 'sense' command is executed. The bits of sense byte 2, when set,

do not cause status indications. The bits have the following meanings assigned:

Bit	*Designation*
0	(Not used)
1	(Not used)
2	Card in primary wait station
3	Card in secondary wait station
4	NPRO allowed
5	Hopper cycle not complete
6	Card in transport counter bit 2
7	Card in transport counter bit 1

Card in Primary Wait Station (Bit 2)

The card in primary wait station bit is set when a card leaves the read station to enter the primary wait station. It is reset to 0 when the card leaves the wait station to enter the punch station. If a card is manually removed from the wait station, the bit is not reset.
Note: The 5425 has no card sensors in its wait stations.

Card in Secondary Wait Station (Bit 3)

The card in secondary wait station bit is set when a card leaves the read station and enters the secondary wait station. It is reset when the card leaves the wait station to enter the punch station. If a card is manually removed from the wait station, the bit is not reset.

NPRO Allowed (Bit 4)

The non-process-runout allowed bit is on whenever the NPRO key is operational. During certain jams, however, some cells in the feed path may be covered by wrongly-positioned cards. In such cases, the NPRO allowed bit is off to indicate that the card path must be cleared by manual intervention before NPRO can be performed.

Hopper Cycle Not Complete (Bit 5)

The hopper cycle not complete bit is set when a command causing a feed cycle is accepted, and is reset when a card has left the hopper for that feed cycle.

Card in Transport Counter Bits 2 and 1 (Bits 6 and 7)

The card in transport counter is incremented when a card leaves the wait station and is decremented when a card is assigned a stacker selection. The counter indicates the number of cards between the wait stations and the stackers. When the transport has come to a complete stop following a feed check, the value of the counter is equal to, or (at most) one greater than, the actual number of cards between the wait stations and the stacker transport but not including cards in the wait stations themselves.

Sense Byte 3

Sense byte 3 contains a hexadecimal number whose value can represent any one of 22 feed checks and emitter checks in the 5425. It is used for error logging and analysis. All checks represented in this byte are 5425 hardstops. All the check conditions (except stacker jam, gear emitter check, and fire CB check) are activated, via a fiber optic bundle, by photo-electric cells in the card path. The state of these cells, in conjunction with timing circuits, enables checks to be recognized when cards are not in their correct positions in the card path. Checks are reset by depression of the NPRO key. Any one of these checks will set the feed check bit in sense byte 1. The checks also light a numbered feed check light on the 5425 operator panel. Values of sense byte 3, check names, and operator panel light numbers are shown in Figure 77.

Hexadecimal Value of Sense Byte 3	Check Name	Operator Panel Light
01	Hopper eject check	1
02	Read inject check	2
03	Read station check	3
04	Read eject check	4
05	Early wait eject check	5
06	Wait eject check	6
07	Punch inject check	7
08	Punch registration check 1	8
09	Punch station check	9
0A	Punch registration check 2	10
0B	Punch transport check	11
0C	Punch eject check	12
0D	Corner station check	13
0E	Corner eject check	14
0F	Print inject check	15
10	Print station check	16
11	Print eject check	17
12	Stacker transport check	18
13	Stacker jam	19
14	Gear emitter check	20
15	Fire CB check	20
16	Cover open check	20

Note: The panel lights marked "A" and "B" are for use by the CE.

Figure 77. 5425 – Checks in Sense Byte 3 [10856]

Hopper Eject Check (01 Hex): The hopper eject check indicates that a card covered the hopper cell late.

Read Inject Check (02 Hex): The read inject check indicates that a card arrived late at the read station.

Read Station Check (03 Hex): The read station check indicates that a card covered the read station cell when no card was expected.

Read Eject Check (04 Hex): The read eject check indicates that a card was late in uncovering the read station cell.

Early Wait Eject Check (05 Hex): The early wait eject check indicates that a card covered the prepunch cell when no card was expected.

Wait Eject Check (06 Hex): The wait eject check indicates that a card was late covering the prepunch cell during a non-punch operation.

Punch Inject Check (07 Hex): The punch inject check indicates that a card was late covering the prepunch cell during a punch operation.

Punch Registration Check 1 (08 Hex): This check indicates that a card was early uncovering the prepunch cell during a punch operation.

Punch Station Check (09 Hex): The punch station check indicates that a card was late uncovering the prepunch cell during a non-punch operation.

Punch Registration Check 2 (0A Hex): This check indicates that a card was late uncovering the prepunch cell during a punch operation.

Punch Transport Check (0B Hex): The punch transport check indicates that a card was late covering the corner cell during a non-punch operation.

Punch Eject Check (0C Hex): The punch eject check indicates that a card was late covering the corner cell during a punch operation.

Corner Station Check (0D Hex): The corner station check indicates that a card was early uncovering the corner cell.

Corner Eject Check (0E Hex): The corner eject check indicates that a card was late uncovering the corner cell during a non-print operation.

Print Inject Cell (0F Hex): The print inject check indicates that a card was late uncovering the corner cell during a print operation.

Print Station Check (10 Hex): The print station check indicates that a card was late covering the post-print cell during a non-print operation.

Print Eject Check (11 Hex): The print eject check indicates that a card was early or late covering the post-print cell during a print operation.

Stacker Transport Check (12 Hex): The stacker transport check indicates that a card was late uncovering the post-print cell.

Stacker Jam (13 Hex): This check indicates a stacker jam.

Gear Emitter Check (14 Hex): The gear emitter check indicates that the gear emitter is missing pulses. This condition may require CE attention.

Fire CB Check (15 Hex): The fire CB check indicates that the print fire emitter is missing pulses. This condition may require CE attention.

Cover Open Check (16 Hex): The cover open check indicates that the cover was opened after a command was issued, that is, while cards were in motion, and the motor stopped at random. In such cases, the card path must be cleared by the operator because the NPRO key is probably not operational.

Sense Byte 4

Sense byte 4 defines the card column group and tier where the error was detected which caused the first read check or punch check of a card cycle. If more than one read check or more than one punch check occurs during a card cycle, a multiple check indicator in sense byte 4 will be set. The read check (bit 0) and punch check (bit 1) bits in sense byte 1 show whether sense byte 4 contains read check or punch check information. In the unusual case where a read check and a punch check occur during the same card cycle, bits 0 and 1 will both be set in sense byte 1, which means that the contents of sense byte 4 will be undefined.

Figure 78 shows how sense byte 4 defines whether a single error or multiple errors occurred and, if a single error, the tier and column group in which the error was detected.

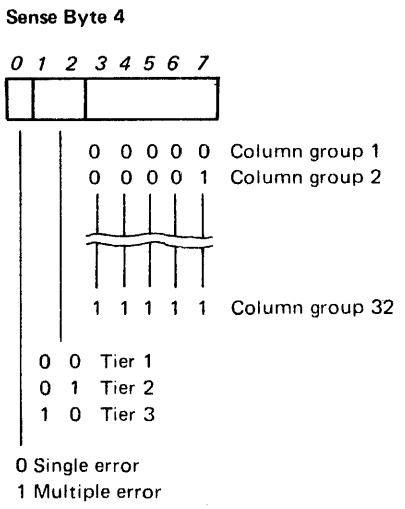


Figure 78. 5425 – Functions of Sense Byte 4 [10857]

Sense Byte 5

Sense byte 5 specifies the row or rows for the tier and column identified in sense byte 4 in which a read check or punch check error occurred. Thus, sense bytes 4 and 5 together define the position of the error which caused the first read check or punch check during a card cycle down to one or more of the 24 read cells or punches or their associated circuits. The bits in sense byte 5 have the following meanings assigned:

Bit	*Designation*
0	D row miscompare
1	C row miscompare
2	B row miscompare
3	A row miscompare
4	8 row miscompare
5	4 row miscompare
6	2 row miscompare
7	1 row miscompare

Sense Bytes 6, 7, 8, 9, and 10

Sense bytes 6, 7, 8, 9, and 10 form a table of the five most recent command strings. When a new last command string appears in sense byte 6, the previous contents of sense byte 6 are shifted down to sense byte 7, the previous contents of sense byte 7 are shifted down to sense byte 8, and so on. (A command string starts with the first command following any command causing a feed and ends with the next command causing a feed.)

The bits in sense byte 6 refer to the most recent command string. This command string may not have been carried out completely because of an error condition occurring after acceptance of a command causing one feed but before acceptance of a command causing the next feed. Sense byte 6 contains information about the last command accepted. The bit assignment is the same in each of the bytes (6 to 10).

Bit	*Designation*
0	Secondary
1	Print four lines
2	Stacker select M2
3	Stacker select M3
4	Punch
5	Feed command sample
6	Print
7	Read

Secondary (Bit 0)

If the secondary bit is set, it indicates that the command string applies to the secondary card feed path. If the secondary bit is off, it indicates that the command string applies to the primary card feed path.

Print Four Lines (Bit 1)

The print four lines bit, when set, indicates that four lines were to be printed during the feed operation.

Stacker Select M2 and Stacker Select M3 (Bits 2 and 3)

The stacker select bits indicate the stacker specification for the feed operation in a binary code:

M2	*M3*	*Stacker*
0	1	1
1	0	2
1	1	3
0	0	4

Punch (Bit 4)

The punch bit, when set, indicates that the punch buffer was filled and punching was specified to occur during the feed operation.

Feed Command Sample (Bit 5)

The feed command sample bit, when set, indicates that a feed operation for the command string was initiated.

Print (Bit 6)

The print bit, when set, indicates that a print buffer was filled and printing was specified to occur during the feed operation.

Read (Bit 7)

The read bit, when set, indicates that reading was specified to occur during the feed operation.

5425 ERROR RECOVERY

The following paragraphs describe the action which the operating system should take when errors or unusual conditions which cause an interruption occur in the 5425. The reason for the interruption is shown in the CSW. Any status information other than channel end, device end, and busy indicates an error or unusual condition.

Unit Check in CSW

Any errors detected in the 5425 at initial selection, or when channel end or device end is reported, cause the unit check bit to be set in the CSW. The following sense bytes should be examined:

- Sense bytes 0 and 1 for details of the error condition.
- Sense byte 2 for information on the position of cards in the paths.
- Sense bytes 6, 7, 8, 9 and 10 for a command table of the five most recent command strings.

In addition, the punch buffer and the two print buffers contain data from the last write punch command and the last two write print commands. If a 'set ERP mode' command is given, the ensuing commands can retry this data.

When a unit check is detected, the operating system should invoke an error recovery routine to examine the sense information and display a message defining the operator's procedure. After the operator has responded, the error recovery routine should generate and issue a set of commands, then branch back to the next CCW.

The following paragraphs describe how the program can recover from certain types of errors which are indicated by the setting of certain bits in the sense bytes.

Feed Check (Sense Byte 1, Bit 6)

If a feed check occurs, the operating system should examine the sense bytes to determine the error condition, the most recent feed used (primary or secondary), the number of cards in the paths, and the stacker that may have a wrongly stacked card. A message should be displayed which defines the error, the feed in which it occurred, the number of cards to be repositioned, and a stacker number. When the operator has responded, the operating system should generate a sequence of commands which repositions the cards and reads, punches, prints, and stacks them

according to the information obtained from sense byte 2 and the command history table in sense bytes 6, 7, 8, 9 and 10. At the next device end interruption these commands should be executed and the program should exit from the error recovery procedure.

Punch Check (Sense Byte 1, Bit 1)

If a punch check occurs, the operating system should examine the sense bytes to determine the error conditions, the feed most recently used, and the stacker which has erroneously received a card. This information should be displayed to the operator, who will respond to it. At the next device end interruption, a 'sense' command should be given and the relevant card in wait station bit (sense byte 2, bits 2 and 3) examined. If the card in wait station bit is set, a sequence of commands should be given to retry punching and printing of the card in the wait station. If the relevant card in wait station bit is zero, two command sequences should be given, one to fill the wait station, the other to retry punching.

Read Check (Sense Byte 1, Bit 0)

If a read check occurs, the operating system should examine the sense bytes to determine the error conditions and the feed in which the error occurred. This information should be displayed to the operator, who will respond to it. At the next device end interruption, the failing command should be retried.

Print Data Check (Sense Byte 1, Bit 4)

If a print data check occurs, the operating system should examine the sense bytes to determine the error condition, which should then be displayed for the operator to take action. At the next device end interruption, the next command should be given. The print operation is not repeated.

Hopper Check

A hopper check is indicated when, after unit check has been presented at device end time, bit 1 of sense byte 0 and bit 5 of sense byte 1 are both found to be set. The operating system should examine the sense bytes to determine the error condition and the feed in which the error occurred. This information should then be displayed for the operator to take action.

If bit 7 of sense byte 6 is set, indicating that a read operation was specified, the failing command should be retried. If reading was not specified, a control command should be given to fill the wait station. The next command should then be given.

No Card Available (Sense Byte 0, Bit 6)

The no card available condition is indicated when, after unit check has been presented in the initial status, bit 6 of sense byte 0 is found to be set, but all the check bits in sense byte 1 are zeros. The operating system should analyze the sense bytes to determine the error condition, and the failing command should be examined to determine which feed was in error. A control command should then be given to fill the wait station, and the failing command retried. No message is displayed.

Not-Ready Condition

The not-ready condition is indicated when, after unit check has been presented in the initial status, the intervention required bit (bit 1 of sense byte 0) is found to be set, but all the check bits in sense byte 1 are zeros.

The operating system should examine the sense bytes to determine which of the following conditions has arisen:

Specified feed not ready
Hopper empty
Stacker full
Chip box full or out
Cover open
STOP key has been pressed.

A suitable message should be provided for the operator, and, when he has corrected the condition, the failing command should be given again at the next device end interruption.

Invalid Command or Command Sequence

An invalid command or command sequence is indicated when, after unit check has been presented in the initial status, the command reject bit (bit 0 of sense byte 0) is found to be set, but all the check bits in sense byte 1 are zeros. The operating system should examine the sense bytes to determine the error condition. A suitable message should be displayed for the operator, who should be instructed to terminate the job.

Model 115 Console

The Model 115 console consists of a group of three devices: the video display, the keyboard and the optional IBM 5213 Printer Model 1. For addressing purposes these devices are considered to be one unit (they have a single device address).

The video display and the keyboard function together as the system console (the console is a hardware function, and its operations thus have priority over programmed operations). The commands are executed by the service processor, which operates all parts of the console.

This section describes the commands, status reports, sense information and error recovery procedures for the video display.

Note: Through the remainder of this section the 5213 Printer will be referred to as the console printer.

VIDEO DISPLAY COMMANDS

Command Descriptions

The commands for the video display unit also apply to the optional console printer which operates as a slave device (without identity of its own) in parallel with the video display, if so specified in the program.

The commands are executed by the SVP which operates the hardware front end sections associated with the circuitry of the video display, the keyboard, and the console printer. A transient area in the SVP's control storage serves as a communication area. The data transfer between main storage and the SVP transient area during a 'write', 'erase write', or 'read modified' command is performed in blocks of 128 bytes; the residual length count in the CSW is always reduced by 128.

The commands available for the video display are shown in Figure 79.

Command Code									Command
	CCW Bits								
Hex	0	1	2	3	4	5	6	7	
01	0	0	0	0	0	0	0	1	Write
05	0	0	0	0	0	1	0	1	Erase/write
0F	0	0	0	0	1	1	1	1	Erase all unprotected
06	0	0	0	0	0	1	1	0	Read modified
04	0	0	0	0	0	1	0	0	Sense
03	0	0	0	0	0	0	1	1	Control no-op

Figure 79. Video Display Commands [10858]

Write

The 'write' command provides a means of placing a message on the screen of the video display (and to have this message printed if so desired) without erasing or modifying other messages that may already be displayed on the screen.

The 'write' command causes data transfer in two alternating stages. First, data is transferred from main storage in ascending order of address to the SVP transient area. The data is then transferred from the transient area to the display buffer. This is repeated until the count in CCW bits 48 to 63 is zero or the display buffer is full, whichever occurs first. At that time channel end and device end are indicated if there is no printing. If the message is printed, channel end and device end are indicated when the mechanical print operation is completed.

The transient area serves as a buffer which allows examination of the control characters that are interspersed in the data stream. These control characters determine the location of the text and the cursor on the screen, and they also determine which portions, if any, of the message are to be printed. (For details, see "Video Display Control Characters".)

As the control characters arrive in the transient area, they are examined and the result of this examination controls the data transfer from the transient area to the display buffer. None of the control characters (except attribute characters) are transferred to the display buffer. Each attribute character occupies a display buffer position but is not visible on the screen. The attribute character describes the extent and characteristics of the associated field (such as whether a field is retrievable, can be printed, or is protected from overwriting).

The screen portion available to the program consists of 12 lines of 56 characters each, allowing a total of 672 bytes (minus the invisible attribute characters) to be displayed. To accommodate the total possible length of a write data stream (text and control characters), a length count of up to 2,048 bytes is valid for a 'write' command. Incorrect length is, however, indicated whenever the display buffer is full before the count is reduced to zero (unless the SLI bit is on).

Erase/Write

The 'erase/write' command provides a means of clearing the video display screen, and replacing the previously-displayed

message or messages with new ones. (The new message can also be printed on the console printer, if available.)

The 'erase/write' command first clears the entire display buffer (even if the contents include protected fields). Then the alternating data transfer from main storage to the transient area, and on to the display buffer, occurs. As the control characters appear in the transient area, they are examined to determine the details of the transfer to the display buffer. At the completion of the last transfer action (or at completion of the print operation) channel end and device end are both presented. The maximum length count for an 'erase/write' command is 2,048 bytes. The screen displays the new message or messages and any screen portion not occupied remains dark. If no new cursor position has been specified, the cursor is located in screen position zero (uppermost line, leftmost position).

Erase All Unprotected

The 'erase all unprotected' command provides a means of clearing certain positions on the screen to provide space for the operator to respond to the operating system or request action by putting a message on the screen.

The 'erase all unprotected' command is of the immediate type, and only the command code is transferred from main storage to the SVP. Channel end and device end are both indicated in the initial status on completion of the command code transfer.

The SVP then resets to zero the modified data tags of all unprotected fields in the display buffer and clears these fields and the associated positions on the screen. The keyboard is unlocked and the cursor is placed at the beginning of the first cleared field. The cursor thus indicates to the operator where his input can be entered on the screen. The attention identifier (if any) is also reset to zero by the command. For details, see "Video Display Control Characters".

Read Modified

The 'read modified' command provides a means of transferring all modified data from the display buffer to main storage. Modified data is any data that the operator has introduced into the display buffer via the keyboard. As data is keyed in, the 'attribute' character of the field into which the operator writes is automatically altered by the setting of the modified data tag bit. The program can also specify messages as modified data by assigning an attribute character with the modified data tag bit set to the written field. Modified fields written by the program are not distinguished from those written by the operator, they are treated alike.

A 'read modified' command can be given at any time, but is usually given after an attention interruption has occurred. The attention interruption occurs whenever the operator has pressed the ENTER or the CNCL (cancel) key on the keyboard. To indicate the reason for the attention interruption, the SVP generates an attention identifier byte; this byte is the first byte of information retrieved by a 'read modified' command. If the CNCL key was pressed, a subsequent 'read modified' command retrieves only the attention identifier (which indicates cancel) without further information. This situation is termed a "short read".

If the ENTER key was pressed, the attention identifier will indicate this and subsequently the SVP microprogram searches the display buffer for set modified data tag bits to identify (and retrieve) modified fields. The same action is performed if the 'read modified' command was given for reasons other than an attention interruption. In this case, the attention identifier indicates that the command was unsolicited (the operator did not press the ENTER or CNCL key). In either case, the search of the display buffer begins at buffer location zero and ends at buffer location 672, which is the last position on the screen. The length count of a 'read modified' command must not exceed 2,048 bytes, otherwise incorrect length is indicated.

If no modified fields are found, the attention identifier byte and the buffer address of the cursor (two bytes) are transferred to main storage. These three bytes are termed the "read heading".

If modified fields are found, the read heading, the buffer address order code, and the buffer address for each field and the text data in each field, are transferred in that order sequentially to the transient area to form the modified data stream. The modified data stream does not contain empty buffer positions or attribute characters.

The modified data stream is then transferred from the transient area to main storage. The transfer begins at the main storage location addressed by CCW bits 8 to 31 and continues in ascending order of address until either the count (CCW bits 48 to 63) has been reduced to zero or the modified data stream ends. At that time, channel end and device end are both set in the CSW. In all other cases, channel end and device end are indicated earlier, when the attention identifier (alone) or the read heading has been transferred.

For further information on the control characters that may accompany the text fields, see "Video Display Control Characters".

Sense

The 'sense' command provides a means of transferring information about errors or unusual conditions to main storage for inspection. A typical use of the 'sense' command is to retrieve the cause or causes of a unit check so that the appropriate recovery action can be initiated. The command causes the sense byte to be stored at the main storage location specified in bits 8 to 31 of the CCW. Incorrect length is indicated whenever the count of a 'sense'

command is more or less than one. The incorrect length indication is suppressed if the SLI flag bit (CCW bit 34) is set. For a detailed description of the sense bytes and their contents, see "Video Display Sense Information".

Control No-Op

The 'control no-op' command performs no function at the video display, but channel end, device end and any other status conditions that may exist at the time are presented in the initial status.

Video Display Control Characters

The control characters and orders in the data streams of 'write' and 'erase/write' commands specify the actual screen location of a message and provide information about the message, such as whether it is protected, unprotected, modified, or to be printed on the console printer. The following text describes the control characters in more detail.

Write-Control Character

The write-control character is the first character in the data stream of every 'write' or 'erase/write' command. This character specifies subcommands associated with the keyboard, the audible alarm, and the (optional) console printer. The meanings of the bits which comprise the write-control character are shown in the following table.

Bit	*Designation*
0	(Not used)
1	(Not used)
2	(Not used)
3	(Not used)
4	Start printer
5	Sound alarm
6	Restore keyboard (and reset attention identifier)
7	Reset modified data tags to zero.

Note: A 'write' or 'erase/write' command may be used for control operations such as sounding the alarm, resetting the keyboard, and so on. In these cases only the write control character need be transferred.

Start Printer (Bit 4): If the console printer is installed, the start printer bit, when set, causes the printer to print out all fields on the screen that have the print bit set in their attribute character.

Sound Alarm (Bit 5): This bit, when set, sounds the alarm which is used to alert the operator to the importance of the message. The alarm sounds for a fixed amount of time and is then silenced automatically. The audible alarm is a standard feature on the video display.

Restore Keyboard (Bit 6): The restore keyboard bit, when set, is used to unlock the keyboard and to reset the attention identifier (created by a previous keyboard operation) to zero.

Reset Modified Data Tag (Bit 7): This bit, when set, resets all modified data tag bits to zero prior to the execution of a 'write' or 'erase/write' command, so that new modified data tags can be written.

Set Buffer Address Order

The set buffer address order is a sequence of three adjacent bytes. The first byte is the set buffer address order code (Hex 11). When this code has been recognized, the next two bytes are assumed to represent the buffer address. The buffer address can range from 0 to 672 (decimal) and specifies where the text data is to be located on the screen. The bits in the two buffer address bytes represent a binary number as follows:

Byte 1

Bit	*Value*
0	(Not used)
1	(Not used)
2	(Not used)
3	1024
4	512
5	256
6	128
7	64

Byte 2

Bit	*Value*
0	(Not used)
1	(Not used)
2	32
3	16
4	8
5	4
6	2
7	1

The buffer address is checked for validity and if it is outside the screen area (beyond 672), the 'write' or 'erase/write' command is terminated with unit check set in the CSW. The data stream transferred via a 'write' or 'erase/write' command may contain as many set buffer address orders as required for text distribution on the screen.

Note: If the data stream does not contain a set buffer address order, the data provided by the command enters the buffer location that currently holds the cursor.

Start Field Order

The start field order consists of two bytes. The first byte is the start field order code (Hex 1D) which indicates that the next byte is to be interpreted as the attribute character. The start field order code follows the buffer address bytes

to open the field. A data stream such as the one transferred by a 'write' or 'erase/write' command may be subdivided into as many fields as necessary by means of the start field order. If each of these fields is to be located in a different area of the screen, they must each be preceded by a set buffer address order, otherwise they are stored (and displayed) sequentially.

Attribute Character

The attribute character is a single byte which describes the characteristics of the field that follows it. The field extends from the attribute character to the next attribute character that follows (if any) or to the buffer end.

The attribute character is protected by cursor movement from overwriting by the operator. The program can, however, overwrite any attribute character by use of the 'write' or 'erase/write' command.

The attribute character occupies a buffer position but is not displayed. Because the video display operates in formatted mode only and cannot wrap around, buffer position zero must contain an attribute character.

Each bit in the attribute character, when set, has a specific function. When a bit is zero, it represents the opposite function. The bit assignments are shown in the following table:

Bit	*Assignment*
0	Print
1	Always set (for compatibility)
2	Protected data
3	(Not used)
4	(Not used)
5	(Not used)
6	(Not used)
7	Modified data

Print (Bit 0): The print bit, when set, specifies that the field covered by the attribute character is enabled for printing on the (optional) console printer.

Protected Data (Bit 2): The protected data bit, when set, specifies that the data in the field is to be protected against overwriting by the operator. This protection is required because the operator can move the cursor to any location on the screen via the cursor positioning keys and can thus inadvertently destroy a message. Data fields thus protected cannot be erased by an 'erase all unprotected' command.

Modified Data (Bit 7): The modified data bit, when set, specifies that the field is to be made available for retrieval via a 'read modified' command. Data entered by the operator via the keyboard will always have the modified data bit set. A field that has this bit off is ignored by the 'read modified' command. An 'erase all unprotected' command resets the modified data bits of the attribute characters of all unprotected fields to zero so that none of these fields can be read by a 'read modified' command.

Insert Cursor Order

The insert cursor order consists of one byte (containing hex code 13) that causes the cursor to be relocated to the next available buffer position when the order is detected in the data stream. A data stream may contain as many insert cursor orders as required and each of them causes the cursor to be moved to the current (next) buffer address.

Attention Identifier

The attention identifier is a byte generated by the SVP when the ENTER key, CNCL key or REQ key is operated, or when an unsolicited 'read modified' command is given. The attention identifier interprets the meaning of the attention status (bit 32 in the CSW) so that the operating system can react accordingly. If the operating system issues a 'read modified' command upon detection of the enter or cancel key code, this command is solicited. If the operating system "volunteers" a 'read modified' command, then the command is unsolicited. The attention identifier is generated as follows:

Byte Value (hex)	*Meaning*
7D	ENTER key depressed
6E	CANCEL key depressed
60	No operator action (unsolicited 'read modified')

Once the attention identifier has been generated, it is stored in the SVP. The next 'read modified' command receives the attention identifier as the first byte of the data stream that is transferred to main storage. The identifier is not reset to zero by this read operation, but is reset by the next 'erase all unprotected' command or a 'write' or 'erase/write' command which specifies restore keyboard in its write control character.

VIDEO DISPLAY STATUS INFORMATION

The following paragraphs describe the unit status and channel status reports for the video display, keyboard and optional console printer.

Unit Status

The unit status is recorded in bits 32 to 39 of the CSW. The bits are assigned as follows:

Bit	*Designation*
32	Attention
33	Status modifier
34	Control unit end
35	Busy
36	Channel end
37	Device end
38	Unit check
39	Unit exception

Attention (Bit 32)

The attention bit may be set alone (for an attention interruption) or in the initial or the ending status for a command, depending on the time of the action which caused it to be set. The attention bit is, however, always indicated at the earliest possible moment.

There are two possible causes for the attention bit being set. The operating system should, therefore, give a 'read modified' command. The first byte transferred to main storage will indicate the reason for the attention interruption as follows:

Byte Value (hex)	*Meaning*
7D	ENTER key depressed
6E	CNCL key depressed

7D means that the operator has depressed the ENTER key to enter a message into the display buffer.
6E is solely interpreted by the operating system.

Status Modifier (Bit 33)

The status modifier bit is set together with the busy bit when the video display is addressed while the SVP is occupied by log operations, or manual operations (such as alter/display).

Control Unit End (Bit 34)

The control unit end bit is set when log operations or manual operations have been completed and the display was addressed while such operations were in progress. Control unit end thus signals to the operating system that the display is available.

Busy (Bit 35)

The busy bit, when set, indicates that the video display (or the optional console printer) is either executing a previously-initiated command or has an interruption condition (such as device end or attention) pending. If busy is set together with the status modifier bit, the SVP is occupied with log operations. The setting of control unit end will then indicate when the display is available.
Note: The busy bit is not set when the keyboard is being used because the display system is available.

Channel End (Bit 36)

The channel end bit, when set, indicates that data transfer between main storage and the transient area, or the command transfer, has been completed.

Device End (Bit 37)

The device end bit, when set, indicates that the device is free to execute another command. The term device applies to the video display and the console printer (if installed) but *not* to the keyboard. If the console printer is installed, the setting of device end may also indicate that the console printer has been put manually into the ready state.

Unit Check (Bit 38)

The unit check bit can be set by several errors or unusual conditions, such as incomplete control codes, invalid buffer address specification or equipment check. If unit check is set, a 'sense' command should be given in order to retrieve the actual cause (see "Video Display Sense Information").

Unit Exception (Bit 39)

The unit exception bit is set when print operations are stopped because the MODE SEL key has been pressed.

Channel Status

The channel status is recorded in bits 40 to 47 of the CSW. The bits are assigned as follows:

Bit	*Designation*
40	Program-controlled interruption
41	Incorrect length
42	Program check
43	Protection check
44	Channel data check
45	Channel control check
46	Interface control check
47	Chaining check (not used)

The channel status bits have the same standard functions for the video display as for any device attached via a channel, integrated adapter, or integrated attachment. These functions are described for the 2560 under "2560 Status Information" in the section "IBM 2560 Multi-Function Card Machine; Models A1 and A2". For a more detailed description of the channel status bits, see *IBM System/370 Principles of Operation,* GA22-7000.
Note: Incorrect length is indicated if the length count for a 'read modified', 'write', or 'erase write' command exceeds 2,048 bytes

VIDEO DISPLAY SENSE INFORMATION

The SVP provides only one byte of sense information for the video display.

Sense Byte 0

The bits in sense byte 0 have the following assignments:

Bit	*Designation*
0	Command reject
1	Intervention required
2	(Not used)
3	Equipment check
4	(Not used)
5	(Not used)
6	(Not used)
7	Operation check

Command Reject (Bit 0)

The command reject bit is set when an unassigned command is received at the SVP.

Intervention Required (Bit 1)

The intervention required bit is set only when the optional console printer is installed and either has an end-of-forms condition or the cover is open while an operation that includes printing is attempted.

Equipment Check (Bit 3)

Equipment check is set only when the console printer is installed and a hardware malfunction occurs during a printer operation. Malfunctions of this type are either a failure to reset to a defined state, a failure to send request pulses during a print operation, or a parity error.

Operation Check (Bit 7)

The operation check bit, when set, indicates that one of the following conditions has been detected at the time channel end or device end was presented:

1. An illegal buffer address was detected in the data stream of a 'write' or 'erase/write' command. An address above 672 (decimal) is illegal.
2. A valid buffer address is used but the buffer limits are exceeded during command execution. This can occur if the length count is valid but larger than the space available from the buffer address to the buffer end.
3. An incomplete start field order or an incomplete set buffer address order has been detected in the data stream of a 'write' or 'erase/write' command.
4. Location zero in the display buffer does not contain an attribute character.

Note: An operation check condition is detected during byte transfer from the SVP transient area to the display buffer. The residual length count in the CSW does not show which data byte caused the operation check, because the data is transferred in 128-byte blocks from main storage to the SVP transient area.

VIDEO DISPLAY ERROR RECOVERY

Programming faults, such as those indicated in the sense byte, are the most frequent cause of errors in the video display. Such faults require program debugging. Errors associated with the optional console printer are usually caused by conditions such as end-of-forms or open cover. Both of these conditions render the printer not ready and, thus, require manual intervention by the operator.

If the execution of a command is halted by conditions such as channel data check or channel control check, the command should be retried (retry is frequently successful in these cases). If a 'hard' SVP error occurs (as indicated by the SVP error lamp on the console) the error is not recoverable and initial microprogram loading (IMPL) is required or the CE must be called.

If channel data check or channel control check is indicated, the operating system should find out whether a limited channel logout has been stored at location 176. This logout will show how far the operation has progressed and/or how it was terminated.

Teleprocessing facilities are available for the Model 115 through the optional integrated communications adapter, which enables communication between the system and communication terminals and/or other computers at remote locations.

This chapter briefly outlines the capabilities of the ICA, then goes on to describe the available line control procedures. The characteristics, commands, status reports and sense information for each line control procedure are also described.

Integrated Communications Adapter

The Model 115's integrated communications adapter performs all the functions of, and is equivalent to, a byte multiplexer channel with a maximum of 12 subchannels. Each subchannel consists of a line attachment that provides the necessary control functions for the connected communication line. Five synchronous lines (U.S.A. only), or four synchronous lines and eight asynchronous lines, may be attached. A suitable modem is required for each line (except telegraph lines). Figure 80 shows the types of lines that can be served by the ICA.

Six different line control procedures may be used, in any combination. Each is designed to match the characteristics of the communications terminal equipment on the other end of the line. The following types of line control procedure are available:

IBM Terminal Control – Type 1
IBM Terminal Control – Type 2
Telegraph Terminal Control – Type 1
Telegraph Terminal Control – Type 2
World Trade Leased Telegraph Line Control
Binary Synchronous Communication Control.

To avoid confusion caused by similarities or minor differences between certain types of terminal controls, the remainder of this chapter is divided into six sections. The sections describe the characteristics, available commands, status reports, and sense information for each line control procedure.

IBM TERMINAL CONTROL – TYPE 1

Characteristics

The command set, line control characters, and transmission code comprising the IBM terminal control – type 1 are designed for asynchronous start/stop communication with the following terminals and data communication systems:

IBM 1050 Data Communication System (using 6-bit BCD with shift)
IBM 1060 Data Communication System (using 6-bit BCD without shift)
IBM 2740 Communication Terminal (using 6-bit BCD or EBCDIC with shift)
IBM 2741 Communication Terminal (using 6-bit BCD or EBCDIC with shift).

Note: In the following text, "Type 1 terminals" is used as a summary name to avoid listing all the individual terminals that can be operated by the same line control procedure.

Line Control Characters

Six line control characters are used for type 1 terminals.

Ⓑ *(End of Block):* The Ⓑ ("circle B") character indicates the end of a block of text.

Ⓒ *(End of Transmission):* The Ⓒ character indicates the end of a transmission or the beginning of either a polling or a selection operation.

Ⓓ *(End of Address):* The Ⓓ character indicates the end of an address (if any) and, consequently, the beginning of text. It is a positive response to polling.

Ⓝ *(Negative Response):* The Ⓝ character indicates for polling that the terminal has nothing to send, or for addressing that the terminal cannot receive (or has detected a transmission error).

Ⓢ *(Start of Address):* The Ⓢ character indicates that a message is available for the printer (used only during addressing and concerns the remote station only).

Ⓨ *(Positive Response):* The Ⓨ character indicates that the addressed terminal is ready to receive.

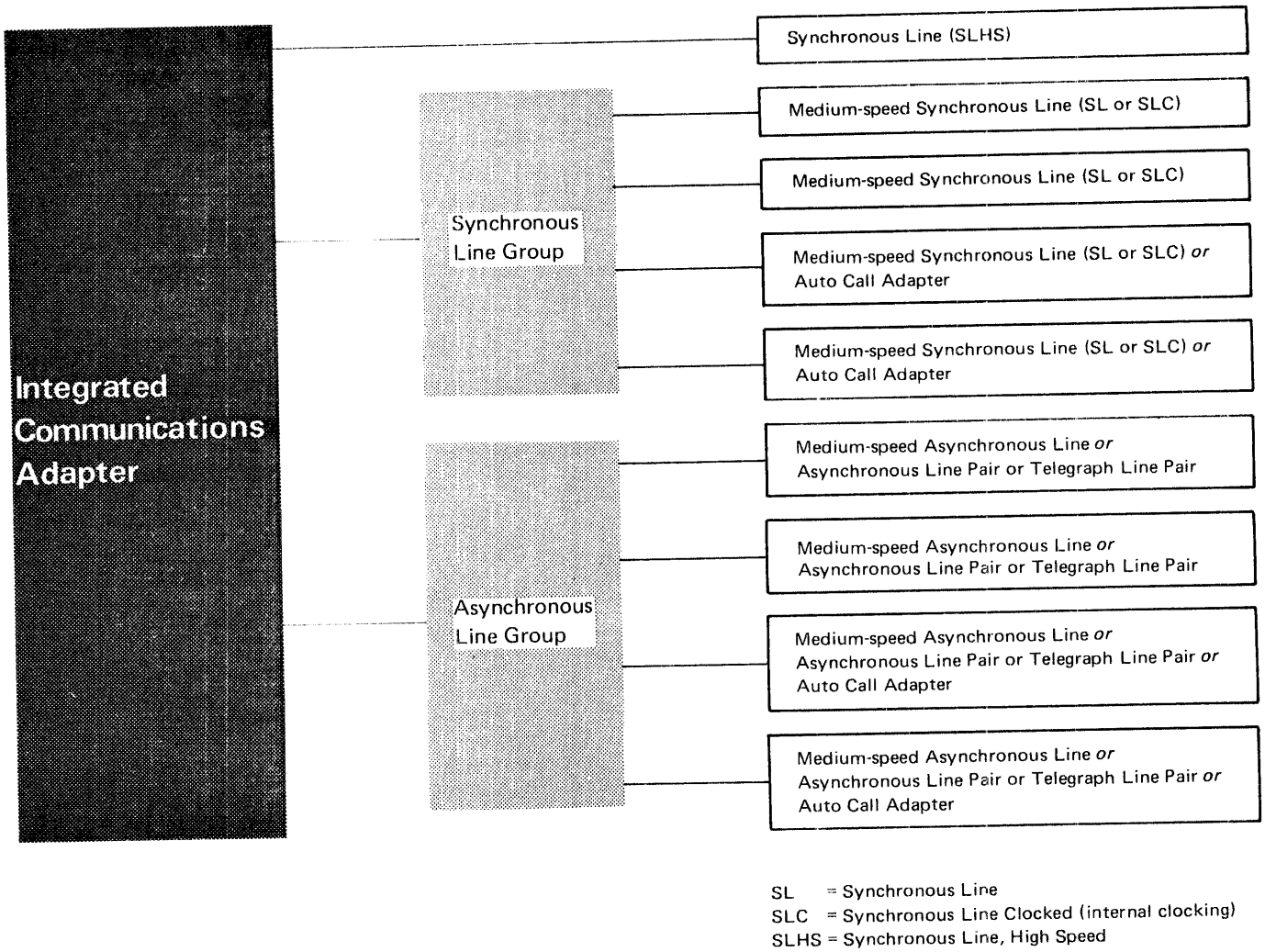
Note: For a listing of all applicable function and control characters, see "Appendix A. ICA Code Tables".

Transmission Code

The transmission code for type 1 terminals is six-bit BCD, also known as the paper tape transmission code (PTTC). The code is shown in the following table.

Storage byte:	0	1	2	3	4	5	6	7	
Interpreted as:	S	B	A	8	4	2	1	C	
Transmission code: start		B	A	8	4	2	1	C	stop

The S-character is the shift bit, which indicates upper case



ICA Overview Configurator

Figure 80. ICA Overview Configurator [10859]

when set, lower case when zero. During transmission, the line attachment inspects the shift bit of each character before it is stripped off. The inspection shows whether or not the shift bit is the same as that of the preceding character. If a shift change is detected (a change from upper case to lower case, or vice versa), the line attachment generates an appropriate shift character (upshift or downshift) which is transmitted ahead of the character that caused the shift change. This allows the remote terminal to operate its shift mechanism.

When the line attachment is receiving, it inspects incoming shift characters but does not transfer them to main storage. The character that follows the shift character is stored with a shift bit that reflects the change effected by the shift character. The start and stop bits are added for transmission and deleted upon reception.

Commands

Figure 81 shows the commands available for type 1 terminals.

Hex	Command Code *CCW Bits* 0 1 2 3 4 5 6 7	Command
02	0 0 0 0 0 0 1 0	Read
01	0 0 0 0 0 0 0 1	Write
0A	0 0 0 0 1 0 1 0	Inhibit
06	0 0 0 0 0 1 1 0	Prepare
27	0 0 1 0 0 1 1 1	Enable
2F	0 0 1 0 1 1 1 1	Disable
29	0 0 1 0 1 0 0 1	Dial
0D	0 0 0 0 1 1 0 1	Break
09	0 0 0 0 1 0 0 1	Poll
03	0 0 0 0 0 0 1 1	Control no-op
04	0 0 0 0 0 1 0 0	Sense
2B	0 0 1 0 1 0 1 1	Set line mode

Figure 81. Commands for Type 1 Terminals [10860]

Read

The 'read' command causes data to be transferred from the addressed line to the main storage address specified in CCW bits 8 to 31. Data transfer continues in ascending order of this address. To ensure that data is actually received on the line, a three-second timeout is started when a 'read' command is given. If the time elapses before data is received, the 'read' command ends with unit check (bit 38 in the CSW) set and the timeout complete bit is set in sense byte 0. If a character is received before the three-second timeout has elapsed, a 28-second timeout is started for each subsequent character.

The data received is normally in the form of a stream that consists of line control characters and text characters. The operations within the ICA and the way in which the 'read' command is terminated depend on the data received, as described in the following text.

Ⓓ Received: If a Ⓓ is received, it is recognized as a line control character if the line attachment is in control mode (the line attachment is in control mode after enable, disable, or end of transmission). Recognition of a Ⓓ causes the line attachment to set text-in and lower case modes. The data that follows Ⓓ will be text.

In text-in mode, when the next incoming character is received, the line attachment begins to accumulate the longitudinal redundancy check character. Each text character received causes the LRC to be updated. Reception continues as long as successive text characters arrive within 28 seconds. All characters are stripped of their start bit and stop bits (these bits do not enter main storage). Shift bits are inserted into the byte prior to storing the byte into main storage.

In text-in mode, further Ⓓ, Ⓝ or Ⓨ characters are not recognized as line control characters, but are treated as text characters.

The read operation continues until a timeout (28 seconds elapsed) occurs, a Ⓑ or Ⓒ is received, or the length count is exhausted, whichever occurs first.

Delete or Idle Characters Received: If delete characters (BA8421C) or idle characters are received, they are included in the LRC accumulation, but are not transferred to main storage.

Shift Characters Received: If a shift character is received it is inspected but not transferred to main storage. The next character received is stored with a shift bit that corresponds to the shift change effected by the shift character. The shift character is included in LRC accumulation.

Ⓑ Received: Receipt of Ⓑ indicates that the end of the text block has been reached and the line attachment stops LRC accumulation. The next character received is assumed to be the LRC character from the remote terminal. This LRC character is compared with the LRC accumulated in the line attachment and if both are the same, channel end and device end are presented for the 'read' command. The attachment remains in text-in mode.

Ⓒ Received: Receipt of Ⓒ indicates the end of transmission, and channel end, device end and unit exception (bits 36, 37, and 39 in the CSW) are presented to terminate the 'read' command. The line attachment goes back to control mode and lower case mode.

Timeout: If a timeout elapses, the 'read' command ends with channel end, device end, and unit check. The timeout complete bit in sense byte 0 will also be set.

Write

The 'write' command causes data from the main storage location specified in CCW bits 8 to 31 to be transmitted over the addressed communication line. One or more characters can be sent. If more than one character is sent,

the additional characters are taken from main storage in ascending order of address. The action taken by the ICA depends on the data being transmitted, as described in the following text.

Ⓓ *Transmitted:* If a Ⓓ is transmitted, the data that follows (if any) will be text. Transmission of Ⓓ places the line attachment in text-out mode, provided that it was previously in control mode or text-in mode. The Ⓓ also puts the line attachment in lower case mode.

When text-out mode is set, the line attachment begins to accumulate an LRC character. The LRC character is updated with each additional character that is transmitted. Text-out mode causes the shift bit of each text character to be inspected before it is stripped off. If a text character has its shift bit set and the immediately preceding character had its shift bit at 0, the line attachment generates, and transmits, an upshift character. Simultaneously, it sets upper case mode before the next text character is transmitted. If the line attachment detects a change to lower case, the converse happens.

Transmission (writing) continues until a Ⓑ is detected in the output stream or the length count reaches zero, whichever occurs first. Transmission occurs at the speed associated with the addressed line. The line attachment converts the main storage data to the appropriate code (6-bit BCD) and provides the start bit at the beginning and the stop bit at the end of each character.

Ⓒ *Transmitted:* If a Ⓒ is transmitted, the LRC characters are reset in both the line attachment and the receiving station. The 'write' command does not end. (Usually a polling or addressing character follows Ⓒ.)

Ⓑ *Transmitted:* If a Ⓑ is transmitted, LRC accumulation stops and the LRC character is transmitted immediately after the Ⓑ. Then channel end and device end are presented for the 'write' command. Ⓑ is the only character that ends a 'write' command.

Steady Space Level Sensed: If a steady space level for more than 16 bit times is sensed on the receiving line and a 'set mode' command specified "write interruption", the 'write' command ends with unit check, and intervention required is set in sense byte 0.

Notes:

1. The write interruption feature requires a four-wire line.
2. A 'write' command need not necessarily transmit an address and text. Instead it may be used to transmit a positive or negative acknowledgement, such as Ⓨ or Ⓝ.

Polling and Addressing with Alternate Read and Write Commands

'Read' and 'write' commands can be used alternatingly to poll or address type 1 terminals in a multipoint network.

Addressing: Addressing is used to find out if a terminal is ready to receive data. Before addressing can be performed, the line attachment must be in control mode. This can be accomplished by giving a 'write' command that transmits a Ⓒ (end of transmission) followed by the terminal address. The 'write' command must be chained to a 'read' command so that the response can be received as soon as possible. If Ⓝ is received (negative response) the remote terminal cannot receive and the 'read' command ends with channel end, device end, and unit exception set. If a Ⓨ is received, the remote terminal is ready to receive and the 'read' command ends with channel end and device end.

Polling: Polling is used to find out if any remote terminal has a message to send. Before polling can be performed, the line attachment must be in control mode. This can be accomplished by giving a 'write' command that transmits a Ⓒ followed by the polling address. The 'write' command should be chained to a 'read' command to obtain the response as quickly as possible. If a Ⓝ is received, the remote terminal has nothing to transmit and the 'read' command ends with channel end, device end, and unit exception set. If nothing is received before three seconds have elapsed, the command ends with channel end, device end, and unit check. In either case, the line attachment remains in control mode so that polling (or addressing) can continue. If a Ⓓ is received, however, the polled terminal will transmit text. The line attachment therefore goes to text-in and lower case modes, and starts the 28-second timeout for the next character.

Inhibit

The 'inhibit' command is similar to the 'read' command, except that neither a three-second timeout at the beginning nor the 28-second timeouts between characters are started. The 'inhibit' command may be used whenever it is necessary for the line attachment to wait an unlimited period of time for data.

Prepare

The 'prepare' command allows the program to check for meaningful signals on the addressed communication line, and thus find out when a 'read' command should be given. The command is similar to a 'read' although no data is transferred to main storage. When given, the 'prepare' command checks the communication line for a valid start bit. If a valid start bit is detected, the timing circuits next attempt to detect one complete character. If a character can be assembled, channel end and device end are presented for the 'prepare' command. The assembled character, however, is not transferred to main storage.

If no stop bit is found after detection of a start bit and associated character, a 28-second timeout is started. If the timeout elapses before a stop bit is found, the 'prepare'

command ends with unit check and the timeout complete bit is then set in sense byte 0. The lost data bit in sense byte 0, however, is not set, because no data is transferred to main storage during execution of a 'prepare' command.

Enable

The 'enable' command is a prerequisite for data transmission and reception because it enables the addressed line attachment for operation. The command also sets the line attachment to downshift mode. If the 'enable' command is given to a line attachment operating a private or leased line, channel end and device end are set in the initial status. If it is given to a switched line, channel end and device end are set only when the connection with the remote terminal has been established. No data is transferred.

Disable

The 'disable' command makes the addressed line attachment unavailable to commands other than 'enable', 'set line mode' or 'dial'. Other commands issued to a disabled line attachment end with unit check set in the CSW and intervention required set in sense byte 0. If the line to which the 'disable' command is given is a private or leased line, channel end and device end are set in the initial status. If the addressed line is a switched line, a line disconnect occurs and then channel end and device end are presented.

Dial

The 'dial' command can be used only when the addressed line attachment is equipped with the Auto Call Adapter feature and the line attachment is disabled, otherwise the command is rejected. The 'dial' command causes dial digits (which form the subscriber number) to be transferred from the main storage location specified in CCW bits 8 to 31. The transfer continues in ascending order of this address to the automatic calling unit (ACU) until the count in CCW bits 48 to 63 is reduced to zero, or the ACU signals 'abandon call-retry', whichever occurs first. The ACU uses the dial digits to produce dial pulses suitable for the switched network. Channel end and device end are presented for the 'dial' command when the last digit has been transferred and the ACU indicates "connection established". If the connection cannot be made, unit check is set together with channel end and device end and the timeout complete bit is set in sense byte 0. After a 'dial' command, the line attachment is in control mode.

Break

The 'break' command is used to stop transmission from a remote terminal. The 'read' command in progress should be terminated, with a 'halt device' instruction, then the 'break' command can be given. The ICA treats a 'halt device' instruction like a 'halt I/O', so both instructions can be used in the same way. The 'break' command causes a steady space level to be placed on the line for a duration that is determined by the count in CCW bits 48 to 63. The count causes an appropriate number of bytes to be fetched from main storage for timing purposes. These bytes may contain any bit pattern because they are not transmitted over the line. When the count is reduced to zero, channel end and device end are presented.

Note: The 'break' command must only be used if the remote terminal is equipped with a receive interrupt feature, which allows detection of the 'break' signal. For this reason, use of the 'break' command for type 1 terminals can be specified via the 'set line mode' command (set read interruption). If its use is prohibited, a 'break' command is rejected.

Poll

The 'poll' command allows the program to search a multipoint network for remote terminals which have a message to transmit. The 'poll' command provides an automatic procedure that relieves the program from having to give alternate 'read' and 'write' commands.

The 'poll' command causes data to be transferred from the main storage location specified in CCW bits 8 to 31 to the addressed communication line. The data thus transmitted is a 'polling character sequence', which usually consists of a character that sets control mode, terminal address, and a character that specifies an I/O device such as a card reader or card punch (if any) at the remote station.

After transmission of the polling characters, the line attachment is put into receive status until either a reply is received or a timeout occurs. If a negative response, such as a Ⓝ, is received, the next polling character is fetched from main storage and transmitted over the line. The line attachment again checks for a reply. This continues until the polling list is exhausted (all polling characters have been transmitted and the length count reaches zero). The command will then be terminated with channel end and device end set. At this point it is recommended to branch back to the 'poll' command via a 'TIC' command to keep a "polling loop" running until a reply is received.

If a timeout occurs before a reply is received, channel end, device end, and unit check are presented. If, however, a Ⓓ is received, the 'poll' command ends with channel end, device end, and the status modifier (bit 33) set in the CSW. If command chaining has been specified, the current CCW address is incremented by 16 and the CCW at this location is fetched (this should be a 'read' because Ⓓ indicates that a message will arrive). The first character thus read in will be the index character (which is excluded from LRC accumulation). The index character identifies the terminal from which the message is being received.

Control No-Op

The 'control no-op' command performs no function at the line attachment. Channel end, device end, and any other status conditions that may exist at that time are presented in the initial status.

Notes:

1. The 'sadzero', 'sadone', 'sadtwo', and 'sadthree' commands used by the IBM 2703 Communication Control are accepted by the Model 115's ICA, but are treated as 'control no-op'.
2. The 'auto-wrap' command used by the System/360 Model 25 is rejected if given to the Model 115's ICA.

Set Line Mode

The 'set line mode' command provides a means of adjusting the line attachment to suit the characteristics of the communications system with which it is used. Certain details, such as the availability of a two-wire or four-wire line, or the availability of a duplex or half-duplex modem, may not be known or may be uncertain up to the point of actual installation. The 'set line mode' command, therefore, allows the programmer to specify the characteristics of remote terminals which will communicate with the ICA so that there is no need for hardware changes. The following information can be specified in one byte that is transferred from the main storage location designated in CCW bits 8 to 31 to the line attachment.

Bit	*Meaning*
0	Continuous request to send
1	Leased line (0)/switched line (1)
2	(Not used)
3	Unit exception suppress or downshift on space
4	Read interruption
5	Write interruption
6	(Not used)
7	(Not used)

Information specified by the 'set line mode' command must correctly define the characteristics of the equipment with which the ICA is to communicate. If, for example, leased line is specified by bit 1 but a switched line is actually used, correct operation will be impossible although no error indication will be given.

The following text describes in more detail the conditions that can be specified by the 'set line mode' command.

Continuous Request to Send (Bit 0): Bit 0, when set, specifies that the 'request to send' circuit to the modem is on at all times that the line attachment is enabled. Normally, request to send is set only when a 'write', 'break', or 'poll' command is given and this causes a short delay until 'clear to send' is returned. Continuous request to send avoids turnaround delays but requires a duplex line.

Leased Line/Switched Line (Bit 1): When bit 1 is off (0), leased line is specified; when bit 1 is set, switched line is specified.

Unit Exception Suppress (Bit 3): When bit 3 is set, unit exception status is suppressed in all cases where it would normally be given (such as a Ⓒ received). The suppression of unit exception must be specified when a 2741 terminal is attached to the other end of the line. Because the downshift on space function is not applicable, bit 3 only serves as the unit exception suppressor.

Read Interruption (Bit 4): When bit 4 is set, a 'break' command is not rejected (as it normally would be) but is executed. This allows the program to stop a remote terminal that forces the line attachment to continue reading. The 'read' command must, however, be terminated (via 'halt I/O') before the 'break' command can be given. Bit 4 should be set only if the remote terminal is capable of recognizing a 'break' signal.

Write Interruption (Bit 5): When bit 5 is set, the line attachment is capable of recognizing a 'break' signal received from the remote terminal while the attachment is transmitting to this terminal. The remote terminal operator is thus allowed to press a break key or attention key to stop execution of the 'write' command.

Default Values of 'Set Line Mode' Command: If no 'set line mode' command is given, the following modes of operation are effective:

1. Not continuous request to send
2. Leased line
3. Not unit exception suppress
4. No read or write interruption.

Sense

The 'sense' command causes sense information to be transferred from the line attachment to main storage for inspection. A 'sense' command can be given at any time but should always be given when unit check is set in the CSW. For details of the sense information available for type 1 terminals, see "Sense Information" in this section. Channel end and device end are set when transfer of the sense information to main storage is complete.

Unit Status

The unit status shows the state of the addressed line attachment (which works as a subchannel). The unit status is recorded in bits 32 to 39 of the CSW. The bits have the following assignments:

Bit	*Designation*
32	Attention (not used)
33	Status modifier
34	Control unit end (not used)
35	Busy
36	Channel end
37	Device end
38	Unit check
39	Unit exception

Attention (Bit 32)

The attention bit is not used.

Status Modifier (Bit 33)

The status modifier bit is set (together with channel end and device end) when a 'poll' command ends because a Ⓓ is received from the polled terminal. The Ⓓ indicates that text will follow. If command chaining is in progress, the status modifier causes the current CCW address to be incremented by 16, to indicate the address of the CCW after the next sequential one to be fetched). This should be a 'read' command.

Control Unit End (Bit 34)

The control unit end bit is not used.

Busy (Bit 35)

The busy bit is set if an inline test is running and the subchannel is busy. If a 'start I/O' or 'test I/O' instruction is given, condition code 1 is set in response.

Channel End (Bit 36) and Device End (Bit 37)

The channel end and device end bits are always presented together when the line attachment becomes available for a new command. Depending on the command, this may occur at initial selection or later. Channel end and device end, with or without the status modifier, indicate normal or successful completion of a command. If unit check accompanies this status, a 'sense' command must be given to find the exact circumstances in which the command was completed.

Unit Check (Bit 38)

The unit check bit can be set by several errors or unusual conditions which may have caused the termination of a command. For example, a timeout during a 'read' command or during a 'dial' command sets unit check. An unassigned command; or a command during which a parity error occurs also causes the setting of unit check. A 'sense' command must be given to retrieve the actual error condition. For a more detailed description of the causes of unit check being set, see "Sense Information" in this section.

Unit Exception (Bit 39)

The unit exception bit, when set, indicates either a specific response or a situation that is unexpected. The meaning of unit exception is specific for each of the following commands:

1. For 'write' and 'poll' commands, unit exception indicates that the line was receiving at the time the command was issued.
2. For a 'read' or 'inhibit' command, unit exception indicates that a Ⓒ (end of transmission) or Ⓝ (negative response for polling/selection) has been received.
3. For a 'prepare', 'dial', or 'enable' command, unit exception indicates that the command was ended prematurely by a 'halt I/O' or 'halt device' instruction.

Note: Unit exception is not set when suppressed via a 'set line mode' command.

Sense Information

One byte of sense information is available. The bits in sense byte 0 have the following assignments:

Bit	*Designation*
0	Command reject
1	Intervention required
2	Bus out check (not used)
3	Equipment check
4	Data check
5	Overrun
6	Lost data
7	Timeout complete

Note: All conditions indicated in sense byte 0 set unit check in the CSW.

Command Reject (Bit 0)

The command reject bit is set for any invalid command. Command reject is also set when a 'dial' command is given to a line that does not have the auto call adapter installed or when the 'break' command is given although read interruption has not been specified.

Intervention Required (Bit 1)

The intervention required bit is set whenever the line attachment, the modem, or the automatic calling unit is not ready. The line attachment is not ready when, for example, it has been disabled. The modem is not ready if it fails to indicate 'data set ready' or if it remains in receive mode when it should be in transmit mode (half-duplex modems). The ACU is not operational when its power indicator line is off. The intervention should then consist of issuing an 'enable' command, getting the modem on-line, or turning power on at the ACU, as the case may be. Intervention required is set when a steady down level is received during a 'write' command, provided write interruption was specified in the 'set line mode' command.

Bus Out Check (Bit 2)

The bus out check bit is not used.

Equipment Check (Bit 3)

Equipment check is set if malfunctions are detected within the attachment hardware.

Data Check (Bit 4)

The data check bit is set if a vertical redundancy check or longitudinal redundancy check is detected. The following are examples of situations which can cause data check to be set:

1. Line attachment has been transmitting text, and receives a Ⓝ (indicating that the remote terminal detected a VRC or LRC error).
2. Line attachment is receiving text ('read' command) and receives a character with bad VRC, or the LRC received does not match the locally-accumulated LRC.
3. After execution of a 'poll' command, the line attachment receives a character other than Ⓝ or Ⓓ.

Overrun (Bit 5)

The overrun bit is set when a data byte is lost because data service could not be obtained from the line attachment within one character interval.

Lost Data (Bit 6)

The lost data bit is set when at least one data byte is lost for reasons other than overrun. The following are typical situations which can cause the lost data bit to be set:

1. One complete character (or more) has been received by the line attachment when a 'read' command is given for that line. The character is "unsolicited" and is therefore lost.
2. A 'halt I/O' or 'halt device' instruction stops data reception during execution of a 'read' or 'inhibit' command before the ending status is set.
3. During execution of a 'dial' command, the telephone line is busy or the call is answered before the last dial digit has been transferred.
4. The channel stops during execution of a 'read' command.

Timeout Complete (Bit 7)

The timeout complete bit is set when the period of time within which a character should be received has elapsed before a character was received. The length of the timeout depends on the mode in which the line attachment operates. When in control mode, the first character for a 'read' command must be received before three seconds have elapsed. When in text-in mode, a character must be received before 28 seconds have elapsed. In the case of a 'prepare' command, timeout complete is set when a valid start bit was detected but no stop bit can be found.

IBM TERMINAL CONTROL – TYPE 2

Characteristics

The IBM terminal control – type 2 is designed for communication with the IBM 1030 Data Collection System. The 1030 Data Collection System uses the 6-bit BCD (PTTC) code without shift. The command set and the control characters used are the same as for terminal control type 1, except that there is no 'dial' command or 'break' command.

Line Control Characters

The following line control characters are used with terminal control – type 2.

Ⓑ *(End of Block):* Ⓑ indicates the end of a block of text data.

Ⓒ *(End of Transmission):* Ⓒ indicates end of transmission and sets the line attachment to control mode.

Ⓓ *(End of Address):* Ⓓ indicates the end of an address (if any) and thereby the beginning of text.

Ⓝ *(Negative Response):* Ⓝ indicates that the remote station cannot receive, has nothing to send, or detected a transmission error during reception.

Ⓨ *(Positive Response):* Ⓨ indicates that the remote station is ready to receive or has received error-free data.

Ⓢ *(Start of Address):* Ⓢ indicates that a message is available for the printer (used only during addressing and concerns the remote station only).

Note: For a listing of all applicable control characters, see "Appendix A. ICA Code Tables".

Transmission Code

The transmission code on the line differs in one aspect from that for type 1 terminals. On transmission, the line attachment adds one start bit and two stop bits. Shift bits are not used. There is no LRC accumulation in terminal control – type 2.

The following line transmission code is used in relation to EBCDIC:

Storage byte:	0	1	2	3	4	5	6	7	
Interpreted as:	–	B	A	8	4	2	1	C	
Transmission code:	start	B	A	8	4	2	1	C	stop, stop

Code translation and the addition (or deletion) of start and stop bits are performed within the ICA.

Commands

Figure 82 shows the commands available for type 2 terminals.

Hex	Command Code *CCW Bits* 0 1 2 3 4 5 6 7	Command
02	0 0 0 0 0 0 1 0	Read
01	0 0 0 0 0 0 0 1	Write
0A	0 0 0 0 1 0 1 0	Inhibit
06	0 0 0 0 0 1 1 0	Prepare
27	0 0 1 0 0 1 1 1	Enable
2F	0 0 1 0 1 1 1 1	Disable
09	0 0 0 0 1 0 0 1	Poll
03	0 0 0 0 0 0 1 1	Control no-op
04	0 0 0 0 0 1 0 0	Sense
2B	0 0 1 0 1 0 1 1	Set line mode

Figure 82. Commands for Type 2 Terminals [10861]

Read

The 'read' command causes data to be transferred from the addressed line to the main storage address specified in CCW bits 8 to 31. Data transfer continues in ascending order of this address. To ensure that data is actually being received on the line, a three-second timeout is started when a 'read' command is given. If the character arrives before the three seconds have elapsed, a 28-second timeout is started for each subsequent character. If no data is received before the three seconds have elapsed, unit check is set in the CSW, together with the timeout complete bit in sense byte 0.

For a 'read' command, the operations within the ICA depend on what data is received, as described in the following text.

Ⓓ *Received:* If a Ⓓ character is received while the line attachment is in control mode (which it is after end of transmission, disable, or enable) the attachment sets text-in mode. In text-in mode, further Ⓓ, Ⓝ, or Ⓨ characters are not recognized as line control characters, they are treated as text characters. No LRC accumulation takes place, but each character is individually checked for odd VRC.

Delete Characters or Idle Characters Received: If delete characters (BA8421C) or idle characters (B8421) are received, they reset the timeout but are not transferred to main storage.

Ⓑ *Received:* If a Ⓑ is received, channel end and device end are presented for the 'read' command. The line attachment remains in text-in mode.

Ⓒ *Received:* If a Ⓒ is received, channel end, device end, and unit exception are set in the CSW. The line attachment goes back to control mode.

Timeout: If a timeout occurs, the 'read' command ends with channel end, device end, and unit check set, and the timeout complete bit is set in sense byte 0.

Write

The 'write' command causes data from the main storage location specified in CCW bits 8 to 31 to be transferred (in ascending order of this address) to the selected communication line. The storage bytes are translated to six-bit BCD and each byte is provided with one start bit and two stop bits. Upon reception these bits are deleted by the remote station. The action taken by the ICA during write operations depends on what is being transmitted, as described in the following text.

Ⓓ *Transmitted:* If a Ⓓ is transmitted, the line attachment sets text-out mode, provided that it was in text-in or control mode at the time Ⓓ was sent. No LRC accumulation takes place.

Ⓒ *Transmitted:* If a Ⓒ is transmitted, the line attachment goes into control mode. The 'write' command does not end (Ⓒ is normally followed by a polling or addressing character sequence).

Ⓑ *Transmitted:* If a Ⓑ is transmitted, channel end and device end are presented for the 'write' command. The line attachment remains in text-out mode.

Note: Ⓑ is the only character capable of ending a 'write' command. For this reason, the command length count (held in CCW bits 48 to 63) should be equal to (or greater than) the number of bytes transferred.

Polling and Addressing with Alternate Write and Read Commands

'Read' and 'write' commands can be used alternatingly to poll or address remote stations (similar to the polling and addressing procedures for type 1 terminals).

Addressing: Addressing is used to find out if a remote station is ready to receive data. Before addressing can be performed, the line attachment must be in control mode. This is accomplished by giving a 'write' command that transmits a Ⓒ. Ⓒ may be followed by Ⓢ after which the actual address is transmitted. The 'write' command must be chained to a 'read' command so that the incoming response can be received as soon as possible. If the response is Ⓝ, the remote station cannot receive and the 'read' command ends with channel end, device end, and unit exception set. If the response is Ⓨ, the remote station is ready to receive and the 'read' command ends with channel end and device end only. Chaining may now progress to a 'write' command that sends the text.

Polling: Polling is used to find out if any remote station has a message to send. A 'write' command is used to transmit the polling character sequence. This must occur in control mode which can be ensured by transmitting Ⓒ, then the polling character sequence. The 'write' command must be chained to a 'read' command to obtain a response as quickly as possible. If the response is Ⓓ, the line attachment sets text-in mode and continues to receive. If the response is Ⓝ, the remote station has nothing to send and the 'read' command ends with channel end, device end, and unit exception set. If a timeout occurs, the 'read' command ends with unit check set.

Prepare

The 'prepare' command allows the program to check for meaningful signals on the addressed communication line, so as to find out when a 'read' command should be given. The command is similar to a 'read' but no data is transferred to main storage. When 'prepare' is given, the line attachment checks the line for a valid start bit. If a valid start bit is detected, the line attachment attempts to assemble a complete character. If a complete character can be

assembled, channel end and device end are presented for the 'prepare' command.

If a start bit was detected but no stop bit can be recognized when it is expected, a 28-second timeout is started. The timeout may elapse (in which case unit check ends the command and the timeout complete bit is set in sense byte 0), or a stop bit may be detected (in which case the command ends normally). The lost data bit in sense byte 0 is not set if the timeout elapses, because no data is transferred to main storage.

Inhibit

The 'inhibit' command is similar to the 'read' command except that it is free of timeouts. It may be used whenever there is a justification for waiting an unlimited amount of time for data.

Enable

The 'enable' command causes the addressed line attachment to be enabled for operation, and is a prerequisite for data transmission or reception. When the 'enable' command is given to a private or leased line attachment, channel end and device end are presented at initial selection. When 'enable' is given to a switched line, channel end and device end are presented only after connection with the remote station has been established.

Disable Command

The 'disable' command makes the addressed line attachment unavailable to any command other than 'enable'. When the attachment is disabled, 'read' and 'write' commands are rejected with unit check set and the intervention required bit is set in sense byte 0. When the 'disable' command is given to a private or leased line attachment, channel end and device end are presented immediately. When 'disable' is given to a switched line, the connection is broken and channel end and device end are set before the command is completed.

Poll Command

The 'poll' command provides an automatic polling procedure (instead of alternate 'read' and 'write' commands) which allows the program to search for remote stations, in a multipoint network, that have a message to transmit. The automatic procedure begins with the transfer of the poll character sequence from the main storage location specified in CCW bits 8 to 31 to the addressed line attachment. The attachment transmits the polling sequence, and is then put into receive mode to check for a response. Either a response is received or the timeout (which was started when the polling sequence was transmitted) elapses. If the timeout elapses, channel end, device end, and unit check are presented.

If a Ⓝ response is received, the polled station has no message to send and the line attachment transmits the next polling character and switches again to receive mode. This may continue until the polling list is exhausted (length count is 0) and the 'poll' command is terminated with channel end and device end set. At this point, the program may branch back to the 'poll' command via a 'TIC' command. This action keeps a polling loop running until a response is received. If a Ⓓ response is received, the polled station is about to send text (Ⓓ indicates a successful poll). The 'poll' command then ends with channel end, device end, and the status modifier set in the CSW. If chaining is being performed, the status modifier causes the CCW address to be incremented by 16 where a 'read' command should be located. The 'poll' command should be chained to that 'read' command to avoid loss of data.

Control No-Op

The 'control no-op' command performs no function at the line attachment. Any status conditions which may exist when the command is first given are presented in the initial status.

Set Line Mode Command

The 'set line mode' command allows the line attachment to be adjusted to suit the characteristics of the communication system with which it is to be used. One byte of mode-setting information is transferred from main storage to the attachment, after which channel end and device end are set. The following can be specified:

Bit	*Meaning*
0	Continuous request to send
1	Leased line (0)/switched line (1)
2	(Not used)
3	Unit exception suppress (not used)
4	Read interruption (not used)
5	Write interruption (not used)
6	(Not used)
7	(Not used)

Continuous Request to Send (Bit 0): Bit 0 specifies the operational characteristic of the modem (half-duplex when 0, duplex when 1).

Leased Line/Switched Line (Bit 1): When bit 1 is set to 1, it specifies switched line operation. When bit 1 is off (0), it specifies leased line operation. Leased line operation implies a permanent connection.

Bit 2: Bit 2 is not used, and must be 0.

Unit Exception Suppress or Downshift on Space (Bit 3): Bit 3 is not used, and must be 0.

Read Interruption (Bit 4): Bit 4 is not used, and must be 0.

Write Interruption (Bit 5): Bit 5 is not used, and must be 0.

Sense Command

The 'sense' command causes sense information to be transferred from the line attachment into the main storage location specified in CCW bits 8 to 31. One byte of information is available from terminal control – type 2 line attachments. A 'sense' command can be used to show the exact reason for unit check being set in the CSW. For details of the sense information available for type 2 terminals, see "Sense Information" in this section.

Unit Status

The unit status shows the status of the addressed line attachment, and is recorded in bits 32 to 39 of the CSW. The bits have the following assignments:

Bit	*Designation*
32	Attention (not used)
33	Status modifier
34	Control unit end (not used)
35	Busy
36	Channel end
37	Device end
38	Unit check
39	Unit exception

The circumstances under which the status bits are set are identical to those for terminal control – type 1.

Sense Information

One byte of sense information is available when unit check is set in the CSW. The bits in sense byte 0 have the following assignments:

Bit	*Designation*
0	Command reject
1	Intervention required
2	Bus out check (not used)
3	Equipment check
4	Data check
5	Overrun
6	Lost data
7	Timeout complete.

The sense bits are set in the same circumstances as previously described for terminal control – type 1, except for cases which are not applicable because of the lack of a 'break' or 'dial' command in terminal control – type 2.

TELEGRAPH TERMINAL CONTROL – TYPE 1

Characteristics

Telegraph terminal control – type 1 comprises the command set, line control characters, and transmission code required to operate the following remote terminals:

AT & T* 83 B2 Selective Calling Terminal
AT & T 83 B3 Selective Calling Terminal
Western Union Plan 115A Terminal.

* American Telephone & Telegraph Company.

Line Control Characters

The following line control characters and character sequences are used:

FIGS (Figures): FIGS is an upshift character that is generated by the line attachment when an outgoing data byte with its shift bit off is followed by a byte with its shift bit set. Upon reception, FIGS is deleted, but the shift bit in the next byte which is to be transferred to storage is set if the preceding character was received in lower case mode.

LTRS (Letters): LTRS is a downshift character that is generated by the line attachment when an outgoing data byte with its shift bit set is followed by a byte with its shift bit off. Upon reception, an LTRS character is deleted but the appropriate shift bit is added to the next byte before transfer to storage.

EOM/EOT (End of Message/End of Transmission): EOM/EOT is a sequence that consists of the upper case H character followed by the LTRS character; this sequence indicates message end (transmission end). To ensure that the remote terminal recognizes the sequence, it is recommended that FIGS H LTRS be transmitted (because the FIGS character sets upper case mode).

V (or M) (Verify): V (or M) is a positive response to addressing but a negative response to polling.

EOA (End of Address): EOA has no control power but is used as a programming convention in polling operations.

Note: For a list of all applicable control characters, see "Appendix A. ICA Code Tables".

Transmission Code

The transmission code used with telegraph terminal control – type 1 is the shifted 5-bit Baudot code with 1 start and 1.5 stop bits, as follows:

Storage byte:	0	1	2	3	4	5	6	7
Interpreted as:	–	–	S	1	2	3	4	5
Transmission code:	start,			1	2	3	4	5, stop

Bits 0 and 1 of the storage byte are zeros. Bit 2 represents the shift bit which is 0 for downshift (lower case) and 1 for upshift. The shift bit is inspected and converted to an appropriate shift character by the line attachment.

Commands

Figure 83 shows the commands available for use by telegraph terminal control – type 1.

Read

The 'read' command causes data from the selected telegraph line to be transferred to the main storage location specified in CCW bits 8 to 31; the transfer continues in ascending order of this address if data is actually received on the line. To ensure that data is actually received on the

Hex	Command Code CCW Bits 0 1 2 3 4 5 6 7	Command
02	0 0 0 0 0 0 1 0	Read
01	0 0 0 0 0 0 0 1	Write
0D	0 0 0 0 1 1 0 1	Break
0A	0 0 0 0 1 0 1 0	Inhibit
06	0 0 0 0 0 1 1 0	Prepare
27	0 0 1 0 0 1 1 1	Enable
2F	0 0 1 0 1 1 1 1	Disable
03	0 0 0 0 0 0 1 1	Control no-op
04	0 0 0 0 0 1 0 0	Sense
2B	0 0 1 0 1 0 1 1	Set line mode

Figure 83. Commands for Type 1 Telegraph Terminals [10862]

line, a three-second timeout is started when the 'read' command is given. If no data is received before the three seconds elapse, the command ends with unit check set and the timeout complete bit set in sense byte 0. If data is received before the three-second timeout elapses, a 28-second timeout is started for each subsequent character.

For a 'read' command, the operations within the ICA depend on the data received, as described in the following text.

FIGS Received: If a FIGS character is received, the line attachment switches to figures (numeric) mode. The FIGS character itself does not enter main storage, but it determines the setting of the shift bit in the storage byte of subsequent characters.

LTRS Received: If an LTRS character is received, the line attachment switches to letters (alphabetic) mode if it is currently operating in figures mode. The LTRS character is not transferred to main storage but it determines the setting of the shift bit for subsequent characters.

Note: If the line attachment is already in the mode dictated by an incoming shift character, the shift character has no effect.

V or M Received: If the character V or M is received as the first non-shift character, the 'read' command ends with channel end and device end set (this is a normal ending).

FIGS H LTRS: If the sequence FIGS H LTRS is received, the 'read' command ends with channel end, device end and unit exception set.

Space Character Received: If a space character is received and 'downshift on space' has been specified by the 'set line mode' command, the line attachment switches to letters mode. The incoming space character receives a 0-shift bit before it is transferred to main storage. If the downshift on space has not been specified, the space character is treated as a text character.

Write

The 'write' command causes data to be transferred to the selected telegraph line from the main storage location specified in CCW bits 8 to 31; data transfer continues in ascending order of this address until the count in CCW bits 48 to 63 is reduced to zero.

The data transfer includes the insertion of the start and stop bits and takes place at the speed assigned to the line.

For a 'write' command, the operations within the ICA depend on the data transmitted, as described in the following text.

FIGS Transmitted: The line attachment inspects the shift bit of each character before the character is transmitted. If the line attachment is in letters mode (as after reset, disable, or enable) a character that has its shift bit set causes the attachment to generate automatically a FIGS character. The FIGS is transmitted ahead of the character that caused its generation and the line attachment switches to figures mode.

LTRS Transmitted: If the line attachment is in figures mode and a character has its shift bit off (0), an LTRS character is generated automatically and transmitted ahead of the character that caused its generation. The line attachment is switched back to letters mode.

Space Character Transmitted: A space character transmitted when downshift on space has been specified (via the 'set line mode' command) causes the line attachment to switch to letters mode irrespective of whether the space character has its shift bit on or off. No LTRS character is generated, however.

Echo Check: If transmission and reception occur simultaneously on the telegraph line (due to the telegraph relays being wrongly positioned), an echo check is recognized and this terminates the 'write' command with unit check set, and data check set in the sense byte.

Shift Characters Transmitted: Care must be taken when transmitting shift characters from main storage, because the line attachment does not recognize them as control characters but treats them as text characters. Shift characters are inspected for their shift bits like any other characters and a shift character is generated automatically when the shift bit differs from that part of the preceding character. This causes two shift characters to be transmitted (one from storage, the other from the line attachment).

Note: The 'write' command is not terminated by any control character sent out. Termination is determined by the CCW count only. However, care must be taken that the program does not accidentally cut off the remote terminal by sending the upper case H followed by LTRS; this is taken as the EOT signal at the remote terminal.

Addressing and Polling

Addressing and polling can be performed by alternate 'write' and 'read' commands (there is no separate 'poll' command).

Addressing: Addressing is used to find out if a remote terminal is ready to receive. A 'write' command is used to address the remote terminal and this 'write' command should be chained to a 'read' command to obtain the response as soon as possible. If the response is a V or M character, the remote terminal is ready to receive and the command ends with channel end and device end. Chaining to a 'write' command may then occur. The message should be started off with EOA, then the text should follow, ending with EOM/EOT.

If the upper case H LTRS sequence (EOM/EOT) is received in response to addressing, the remote terminal cannot receive and the 'read' command ends with unit exception.

Polling: Polling is used to find out whether a terminal has a message to offer. A 'write' command should be given to transmit the polling character. To make sure that the terminal recognizes EOM/EOT, the sequence FIGS H LTRS should be sent as EOT. Thereafter chaining to a 'read' command is required to obtain the response. If a V character is received in response, the terminal has nothing to send and the command ends with channel end and device end. If the terminal has data to send, it would answer with EOA, then text, then EOM/EOT.

Break

The 'break' command is used to stop a remote terminal transmitting. This is achieved by placing a continuous space-level on the addressed telegraph line. Before the 'break' command can be given, receive operations must be stopped by a 'halt I/O' instruction. The command fetches data from the main storage location specified in CCW bits 8 to 31 in ascending order of this address until the count in CCW bits 48 to 63 is reduced to zero. Channel end and device end are then presented for the 'break' command. The data bytes fetched are used by the line attachment to control the duration of the 'break' signal. The bytes may have any bit combination because they are not transmitted over the line. The minimum length of the 'break' signal required to disconnect a remote terminal depends on the characteristics of the terminal.

Note: Before the 'break' command is given, a previous 'set line mode' command must have specified read interruption; otherwise, the 'break' command is rejected.

Inhibit

The 'inhibit' command is similar to the 'read' command, except that neither the three-second nor the 28-second timeout is started. The 'inhibit' command may be used whenever it is necessary for the line attachment to wait an unlimited amount of time for data.

Prepare

The 'prepare' command allows the program to check for meaningful signals on the addressed communication line, and thus find out when a 'read' command should be given. The 'prepare' command is, in fact, similar to a 'read', but no data is transferred to main storage. If a FIGS character is received, the 'prepare' command ends with channel end and device end.

Enable

The 'enable' command is a prerequisite for data transmission and reception. The command also sets the line attachment to downshift mode. If the line attachment is not enabled, commands such as 'read', 'write', 'inhibit', and 'prepare' are terminated with intervention required. The 'enable' command ends with channel end and device end set in the initial status.

Disable

The 'disable' command makes the addressed line attachment unavailable to commands other than 'enable' or 'set line mode'. Other commands given to a disabled line are rejected with unit check set in the CSW and intervention required set in sense byte 0.

Control No-Op

The 'control no-op' command performs no function at the line attachment. Channel end, device end, and any other status conditions that may exist at the time the command is given are presented in the initial status.

Set Line Mode

The 'set line mode' command allows the program to adjust the line attachment to suit the characteristics of the communication system with which the attachment is to operate. For this purpose one byte of mode-setting information is transferred from main storage to the line attachment. The 'set line mode' command can specify the following information:

Bit	*Meaning*
0	Continuous request to send (not used)
1	Leased line (0)/switched line (not used)
2	(Not used)
3	Unit exception suppress or downshift on space
4	Read interruption
5	Write interruption (not used)
6, 7	(Not used)

Downshift on Space (Bit 3): When bit 3 is set, a space character received during a 'read' command puts the line attachment in lower case mode. The same occurs when the line attachment transmits a space character during a 'write'

command. The unit exception suppress function is not applicable.

Read Interruption (Bit 4): When bit 4 is set, a 'break' command is executed instead of being rejected as it would be if bit 4 was off.

Sense

The 'sense' command causes sense information to be transferred from the addressed line attachment into the main storage location addressed via CCW bits 8 to 31. A 'sense' command may be given at any time but should always be given when unit check is set in the CSW. The sense information shows the reason for the unit check (see "Sense Information" in this section).

Unit Status

The unit status is recorded in bits 32 to 39 of the CSW. The bits have the following meanings assigned:

Bit	*Designation*
32	Attention (not used)
33	Status modifier (not used)
34	Control unit end (not used)
35	Busy
36	Channel end
37	Device end
38	Unit check
39	Unit exception

Attention (Bit 32)

The attention bit is not used.

Status Modifier (Bit 33)

The status modifier bit is not used.

Control Unit End (Bit 34)

The control unit end bit is not used.

Busy (Bit 35)

The busy bit is set if an inline test is running and the subchannel is busy. If a 'start I/O' or 'test I/O' instruction is given, condition code 1 is set in response.

Channel End (Bit 36) and Device End (Bit 37)

The channel end and device end bits are always presented together when activity in the line attachment is completed. This may be at initial selection time (as is the case with an 'enable' or 'disable' command) or later (as with a 'read' or 'write' command).

Unit Check (Bit 38)

The unit check bit is set whenever errors or unusual conditions are detected which require further definition through the sense information. For example, unit check is set for a 'read' command when the timeout limit has elapsed before a character is received. In that case, the timeout complete bit in sense byte 0 is set to define the reason for the unit check status. Unit check is also set when intervention is required before a command can be executed because the line is disabled, or when an unassigned command is given.

Unit Exception (Bit 39)

The unit exception bit, when set, indicates a specific form of command termination. Unit exception has a specific meaning for each of the following commands:

1. For a 'read' command, unit exception is set when an EOM/EOT sequence is received.
2. For an 'inhibit' command, unit exception is set when an EOM/EOT sequence is received.
3. For a 'write' command, unit exception is set when the command is given to a line that is currently receiving data or has received data since the end of the previous command.
4. For a 'prepare' command, unit exception is set if a 'halt I/O' or 'halt device' instruction was given before any data was received.

Sense Information

One byte of sense information is available. The bits in sense byte 0 have the following assignments:

Bit	*Designation*
0	Command reject
1	Intervention required
2	Bus out check (not used)
3	Equipment check
4	Data check
5	Overrun
6	Lost data
7	Timeout complete

Command Reject (Bit 0)

The command reject bit is set when an unassigned command (such as 'dial' or 'poll') is given to a line operating under telegraph control – type 1. Command reject is also set if a 'break' command is given while read interruption is not specified in the 'set line mode' command.

Intervention Required (Bit 1)

The intervention required bit is set if a command is given while the line is disabled.

Bus Out Check (Bit 2)

The bus out check bit is not used.

Equipment Check (Bit 3)

The equipment check bit, when set, indicates a basic failure within the attachment hardware.

Data Check (Bit 4)

The data check bit is set for a 'read' or 'inhibit' command when a space level is detected on the line at the time reserved for a stop bit (stop bit error). Data check is set for a 'write' command when, during command execution, the line attachment receives an echo check from the line.

Overrun (Bit 5)

The overrun bit is set if a character is lost during execution of a 'read' or 'inhibit' command. This can happen when a data transfer to main storage fails.

Lost Data (Bit 6)

The lost data bit is set when a character is lost for reasons other than overrun. This could occur during execution of a 'read' or 'inhibit' command when at least one character had been received at the time the command was given. When this happens for a 'prepare' command, lost data is *not* set. Lost data is set, however, when a 'read' or 'inhibit' command is terminated by a 'halt I/O' or 'halt device' instruction. The lost data bit is also set if the byte count in the CCW is reduced to zero during the execution of a 'read' or 'inhibit' command.

Timeout Complete (Bit 7)

The timeout complete bit is set when the time allotted for the assembly of one complete character has elapsed. The timeout limits are 3.0 seconds for the first character, and 28.0 seconds for any subsequent characters.

TELEGRAPH TERMINAL CONTROL – TYPE 2

Characteristics

Telegraph terminal control – type 2 is designed to operate synchronous start/stop terminals, such as Common Carrier TWX Models 33/35, that operate over a switched network. These terminals use the eight-level TWX code.

Line Control Characters

Five line control characters are used.

WRU (Who Are You?): The WRU character is a request for station identification. Upon reception of this character, the remote terminal's automatic address generator responds by sending the assigned identification. WRU, when received during a read operation, causes normal termination of the 'read' command.

XON (Transmitter On): The XON character indicates that the remote terminal is ready to transmit. XON causes a 'read' command to end normally (with channel end and device end).

ACK (Acknowledge): The ACK character is a positive reply to a received message. ACK causes normal ending of a 'read' command.

XOFF (Transmitter Off): The XOFF character indicates that the local terminal may transmit. (XON and XOFF are used to avoid contention.) XOFF causes normal ending of a 'read' command.

EOT (End of Transmission): The EOT character indicates that transmission is completed. EOT causes a 'read' command to end with unit exception set in the CSW.

Note: For a list of all applicable control characters, see "Appendix A. ICA Code Tables".

Transmission Code

The following transmission code is used:

Storage byte:	0	1	2	3	4	5	6	7
Interpreted as:	1	2	3	4	5	6	7	8
Transmission code:	start,	1	2	3	4	5	6	7, parity, stop, stop

The start bit and the two stop bits are added by the line attachment upon transmission and are deleted by the remote terminal upon reception. The parity bit is added when the remote terminal is equipped with a parity-checking feature. Parity checking can be programmed by means of the 'translate and test' instruction.

Commands

Figure 84 shows the commands available for telegraph terminal control – type 2.

Hex	Command Code *CCW Bits* 0 1 2 3 4 5 6 7	Command
02	0 0 0 0 0 0 1 0	Read
01	0 0 0 0 0 0 0 1	Write
0D	0 0 0 0 1 1 0 1	Break
0A	0 0 0 0 1 0 1 0	Inhibit
06	0 0 0 0 0 1 1 0	Prepare
2F	0 0 1 0 1 1 1 1	Disable
27	0 0 1 0 0 1 1 1	Enable
29	0 0 1 0 1 0 0 1	Dial
04	0 0 0 0 0 1 0 0	Sense
03	0 0 0 0 0 0 1 1	Control no-op
2B	0 0 1 0 1 0 1 1	Set line mode

Figure 84. Commands for Type 2 Telegraph Terminals [10863]

Read

The 'read' command causes data to be transferred from the addressed line to the main storage location specified in CCW bits 8 to 31. The data transfer continues in ascending

order of this address. To ensure that data is actually received on the line, a 28-second timeout is started with the acceptance of the 'read' command. If a character is received before 28 seconds have elapsed, a further 28-second timeout is started. If no character arrives before the timeout has elapsed, the 'read' command ends with unit check set and the timeout complete bit set in sense byte 0.

As each character is received, the start and stop bits are removed. The operations within the ICA and the way in which the 'read' command ends depend on the characters received.

WRU, XON, ACK, or XOFF Received: If one of these characters is received, the 'read' command ends with channel end and device end.

EOT Received: If EOT is received, the read command ends with channel end, device end, and unit exception.

Delete Characters Received: If delete characters (all 1-bits) are received, they are not transferred to main storage. They do, however, reset the timeout like all other characters.

Write

The 'write' command causes data to be transferred from the main storage location specified in CCW bits 8 to 31 to the addressed communication line. Data transfer continues in ascending order of this address until the count in CCW bits 48 to 63 is reduced to zero or a 'break' signal is detected, whichever occurs first. As the characters are transmitted, they are provided with one start and two stop bits. None of the control characters have any influence on the 'write' command. However, if space levels are detected on the line in place of the stop bits of two successive characters, a 'break' signal from the remote terminal is recognized (although the line is in transmit mode). This situation causes the 'write' command to end with unit check set, and the intervention required bit is set in sense byte 0. Normally, however, the 'write' command ends, with channel end and device end set, when the count in the CCW is exhausted.

Break

The 'break' command causes a continuous space level to be placed on the line for a duration that is determined by the number of bytes specified. These bytes are fetched from the main storage location specified in CCW bits 8 to 31 until the count is reduced to zero, at which time channel end and device end are presented. The bytes may have any bit combinations as they are used for counting purposes only. The length of the 'break' signal depends on the requirements of the remote terminal; usually it should cover at least two character periods to be effective.

Note: Before the 'break' command is given, a previous 'set line mode' command must have specified read interruption; otherwise, the 'break' command is rejected.

Inhibit

The 'inhibit' command is similar to a 'read' command, but no timeouts are started. The inhibit operation ends just as for a 'read' on reception of WRU, XON, ACK, XOFF, or EOT.

Prepare

The 'prepare' command allows the program to check for meaningful signals on the addressed line, and thus to find out when a 'read' command should be given. When the 'prepare' command is given, the line attachment is put into receive mode although no characters are transferred to main storage. The attachment checks for a valid start bit on the line. If found, the line attachment attempts to assemble one character. If no stop bits are detected for this character, a 28-second timeout is started. If the stop bits are detected before the timeout has elapsed, the 'prepare' command ends with channel end and device end. The 'prepare' command ends in the same way if a 'break' signal is detected on the line. However, if the stop bits associated with the character that has been captured are not detected, the 'prepare' command ends with unit check because the timeout expired. The lost data bit is not set, because no data is transferred to main storage.

Enable

The 'enable' command is a prerequisite for data transmission and reception because it makes the line attachment operational. The 'enable' command also sets the line attachment to downshift mode. Channel end and device end are set for the 'enable' command when connection has been established with the remote terminal.

Disable

The 'disable' command makes the addressed line unavailable to all commands other than 'enable', 'set line mode', or 'dial'. After the disable operation, channel end and device end are presented. In the disabled state, all commands except 'enable', 'set line mode', or 'dial' are terminated with unit check set and intervention required is set in sense byte 0.

Dial

The 'dial' command causes data from the main storage location specified in CCW bits 8 to 31 to be transmitted to the automatic calling unit. Transmission continues until the count in CCW bits 48 to 63 is reduced to zero. The data thus transferred represents the subscriber number. Channel end and device end are presented when the call is completed. If the call is abandoned or if the line was receiving at the time the 'dial' command was given, unit exception is set.

Sense

The 'sense' command causes sense information to be

transferred from the line attachment to main storage for inspection. A 'sense' command can be given at any time but must always be given when unit check is set in the CSW, as the contents of the sense byte will show the reason for unit check. (See "Sense Information" in this section.)

Set Line Mode Command

The 'set line mode' command provides a means of adjusting the line attachment to suit the characteristics of the communications system with which it is being used. One byte of mode-setting information is transferred to the attachment. The mode-setting byte can specify the following information:

Bit	*Meaning*
0	Continuous request to send (not used)
1	Leased (0)/switched (1) line
2	(Not used)
3	Unit exception suppress or downshift on space (not used)
4	Read interruption
5	Write interruption
6	(Not used)
7	(Not used)

Downshift on Space and Unit Exception Suppress: Bit 3 is not applicable to telegraph control – type 2 (must be zero).

Read/Write Interruption: Bits 4 and 5 must be set, because read and write interruptions are mandatory in telegraph control – type 2.

Control No-Op

The 'control no-op' command performs no function except that channel end, device end and any other status conditions that may exist at that time are presented at initial selection.

Unit Status

The unit status is recorded in bits 32 to 39 of the CSW. The bits have the following assignments:

Bit	*Designation*
32	Attention (not used)
33	Status modifier (not used)
34	Control unit end (not used)
35	Busy
36	Channel end
37	Device end
38	Unit check
39	Unit exception

Busy (Bit 35)

The busy bit is set if an inline test is running and the subchannel is busy. If a 'start I/O' or 'test I/O' instruction is given, condition code 1 is set in response.

Channel End and Device End (Bits 36 and 37)

Channel end and device end are always presented together when a command has been accepted or terminated. This status is presented upon acceptance of an 'enable' or 'disable' command. All other commands have this status presented on their termination or completion. When channel end and device end are set, it indicates that the subchannel (line attachment) is available for a new command.

Unit Check (Bit 38)

The unit check bit, when set, indicates that a command was terminated by an error or unusual condition. (The exact cause can be determined from the contents of sense byte 0.) Unit check is, typically, set in the following situations:

1. A timeout elapses during execution of a 'read' command.
2. A 'break' signal is detected during execution of a 'write' command.
3. During execution of a 'prepare' command, a start bit is detected but no stop bits.
4. A command is issued to a disabled line attachment.

For further information on the conditions which set unit check, see "Sense Information" in this section.

Unit Exception (Bit 39)

The unit exception bit, when set, has a specific meaning for each of the following commands:

1. For a 'read' command, unit exception is set when EOT (end of transmission) is received.
2. For an 'inhibit' command, unit exception is set when EOT is received.
3. For a 'dial' command, unit exception is set if the addressed line is receiving at the time the command is given, or if the call is abandoned.

Sense Information

One byte of sense information is available. The bits in sense byte 0 have the following assignments:

Bit	*Designation*
0	Command reject
1	Intervention required
2	Bus out check (not used)
3	Equipment check
4	Data check
5	Overrun
6	Lost data
7	Timeout complete

Command Reject (Bit 0)

The command reject bit is set when a command not assigned to telegraph terminal control – type 2 is given (such as a 'poll' command or a 'dial' command if there is no auto-call adapter). Command reject is also set when a 'break' command is given while read interruption is not specified in the 'set line mode' command.

Intervention Required (Bit 1)

The intervention required bit is set in the following situations:

1. A command other than 'enable', 'set line mode', or 'dial' is addressed to a disabled line attachment.
2. The modem or the ACU is not operational.
3. During the execution of a 'read' or 'inhibit' command, the line attachment receives a steady space level for more than 16 bit times (the 'break' signal) from the remote terminal.

Equipment Check (Bit 3)

The equipment check bit, when set, indicates an error or malfunction in the ICA hardware.

Data Check (Bit 4)

The data check bit is set for a 'read' or 'inhibit' command when a space level is detected on the line at the time reserved for a stop bit (stop bit error). The stop bit time is monitored to ensure that the stop bit length is correct.

Overrun (Bit 5)

The overrun bit is set, during execution of a 'read' or 'inhibit' command, when data service could not be obtained in time from the main storage controller, causing a character to be lost.

Lost Data (Bit 6)

The lost data bit is set when a character is lost for reasons other than overrun. This may occur when a 'halt I/O' or 'halt device' instruction cuts off data transfer to main storage at a time when at least one character has already been gated in from the line. Lost data is also set, during execution of a 'dial' command, when the ACU replies before all dial digits have been transmitted. Lost data is not set for a 'prepare' command.

Timeout Complete (Bit 7)

The timeout complete bit is set during a read operation if the 28-second timeout expires before data has been received. This cannot occur during execution of an 'inhibit' command. For a 'prepare' command, timeout complete is set if a valid start bit was found but no stop bit could be detected within 28 seconds.

WORLD TRADE LEASED TELEGRAPH LINE CONTROL

Characteristics

World Trade leased telegraph line control provides the command set, line control characters, and transmission code required to operate World Trade terminals. The term "World Trade terminals" refers to various European teleprinters using a start/stop five-level code with two shifts (letters shift and figures shift) to transfer data over leased, point-to-point, single-current telegraph lines.

Line Control Characters

Four line control characters and sequences are used.

FIGS: FIGS is a shift character indicating upper case.

LTRS: LTRS is a shift character indicating lower case, and is also a motor start signal when transmitted to a teleprinter.

FIGS X: The FIGS X sequence is a response that ends a 'read' command in normal fashion (EOM/EOB function). The X is an identification number or character previously agreed upon between the subscribers.

FIGS Y LTRS: The FIGS Y LTRS sequence is a response that terminates a 'read' command with unit exception (EOT function). The Y is an agreed identification.

nnnn: The four n (X '06') character sequence will end a 'read' command normally (EOM function).

Transmission Code

The transmission code may be either the International Telegraph Alphabet Number 2 or the Figure-Protected Code ZSC3. Both codes use 5 data bits, one start bit and one elongated (1.5) stop bit, as follows:

Storage byte:	0	1	2	3	4	5	6	7
Interpreted as:	–	–	(S)	1	2	3	4	5
Transmission code:	start,	1	2	3	4	5,	stop	

Commands

Figure 85 shows the commands available for terminals operated by World Trade leased telegraph line control.

Hex	Command Code *CCW Bits* 0 1 2 3 4 5 6 7	Command
02	0 0 0 0 0 0 1 0	Read
01	0 0 0 0 0 0 0 1	Write
0D	0 0 0 0 1 1 0 1	Break
0A	0 0 0 0 1 0 1 0	Inhibit
06	0 0 0 0 0 1 1 0	Prepare
03	0 0 0 0 0 0 1 1	Control no-op
04	0 0 0 0 0 1 0 0	Sense
27	0 0 1 0 0 1 1 1	Enable
2F	0 0 1 0 1 1 1 1	Disable
2B	0 0 1 0 1 0 1 1	Set line mode

Figure 85. Commands for World Trade Leased Telegraph Line Control [10864]

Read

The 'read' command causes data to be transferred from the addressed communication line to the main storage location

specified in CCW bits 8 to 31. To ensure that data is actually received on the line, a 28-second timeout is started when the command is given. If no data is received, the command ends with unit check set in the CSW and the timeout complete bit set in sense byte 0. If a character is received, a further 28-second timeout is started for each successive character and data transfer continues in ascending order of the main storage address.

As the characters are received, the start and stop bits are removed. If shift characters are received, they are inspected but do not enter main storage. If a change from upper to lower case, or vice versa, is detected, the shift bits for the following characters are set as indicated by the shift character. If FIGS is received, following characters have their shift bits set to 1 (for upper case); in the same way, LTRS causes shift bits to be reset to 0 (for lower case). The read operation continues until a FIGS X or FIGS Y sequence is received. FIGS X is the EOM/EOB (end of message/end of block) signal, which has been assigned by agreement between the stations, and it causes channel end and device end to be presented for the 'read' command. FIGS Y is the EOT (end of transmission) signal which causes unit exception to be set with channel end and device end. If a 'break' signal is received, the command ends with unit check set in the CSW and data check set in the sense byte.

Write

The 'write' command causes data to be transferred to the communication line from the main storage location specified in CCW bits 8 to 31. Data transfer continues in ascending order of this address. The characters are provided with one start and 1.5 stop bits before they are transmitted. The shift bit of each character is inspected and if there is a change of shift from the preceding to the current character, the FIGS or LTRS character (as appropriate) is generated in the line attachment and transmitted ahead of the data character causing the shift change.

Most European teleprinters, when connected and supplied with power, are always ready to receive. However, some teleprinters do not run continuously, but use a self-generated timeout (generally between 10 and 30 seconds) to switch off their motors if no data is received. To start the remote teleprinter's motor, therefore, a 'write' command should generally begin by transmitting the LTRS character. Because some teleprinters cannot receive until their motors reach normal running speeds, a number of LTRS characters sufficient to cover 1.5 seconds (average) motor start time should follow, after which, message data may be transmitted. The 'write' command does not end with the transmission of any particular character or sequence, but continues until the count in CCW bits 48 to 63 is reduced to zero. Then channel end and device end are presented for the 'write' command.

If the 'write' command is addressed to a line that is receiving data, the command ends with unit exception set. If a 'write' command runs into an echo check, the command ends with unit check set in the CSW and the data check bit set in sense byte 0.

Note: FIGS and LTRS characters may be transmitted from main storage to the remote teleprinter, but they are not recognized as shift characters by the line attachment. They are treated as normal data instead. This means that the shift bits of FIGS and LTRS are inspected and if they differ from those of preceding characters, two shift characters are transmitted (one from the line attachment, the other from storage).

Break

The 'break' command is used to stop transmission from a remote teleprinter by means of a continuous space level that is transmitted by the line attachment. The duration of the 'break' signal is determined by the number of characters (of any type) that are fetched from the main storage location specified in CCW bits 8 to 31 and ascending locations. The characters are used as timing elements, they are not transmitted. Channel end and device end are presented for the 'break' command when the count in CCW bits 48 to 63 is zero.

Note: The read interruption must have been set by a 'set line mode' command before the 'break' command is given, otherwise the 'break' command is rejected.

Inhibit

The 'inhibit' command is similar to a 'read' command, except that no 28-second timeouts are started between received characters. The 'inhibit' command may be used whenever it is necessary for the line attachment to wait an unlimited amount of time between characters received.

Prepare

The 'prepare' command allows the program to check the addressed line for meaningful signals, and thus to determine if a 'read' command should be given. If a valid start bit is found and a complete character including a stop bit is then received, the 'prepare' command ends in the normal way with the presentation of channel end and device end. If the start bit was found but no stop bit was found at stop bit time, a 28-second timeout is started. If the timeout elapses with no stop bit found, unit check is set in the CSW and the timeout complete bit is set in sense byte 0.

Control No-Op

The 'control no-op' command causes no action in the line attachment. Channel end, device end, and any other status conditions that may exist are presented at initial selection.

Sense

The 'sense' command causes one byte of sense information to be transferred from the line attachment to main storage

for inspection. The 'sense' command may be given at any time but should always be used when unit check is set in the CSW, as the information in the sense byte will show the reason for unit check being set (see "Sense Information" in this section).

Enable

The 'enable' command turns on the line attachment and is a prerequisite for transmit and receive operations. The 'enable' command sets the attachment to downshift mode.

Disable

The 'disable' command turns off the line attachment. In the disabled state, all commands except 'enable' and 'set line mode' are terminated with unit check set in the CSW and intervention required set in sense byte 0.

Set Line Mode

Up to three bytes of mode-setting information can be specified, by the 'set line mode' command, for World Trade leased telegraph line control.

Mode Byte 1: Bit 4 (08 hex) must be set, because read interruption is standard to allow the 'break' command to be issued. The other bits must be zeros.

Mode Byte 2: The "X" identifier in the EOM ending sequence can be modified by specifying any lower case character in this byte. The basic X identifier is character G (0B hex).

Mode Byte 3: The "Y" identifier in the EOT ending sequence can be modified by specifying any lower case character (except the X identifier) in this byte. The basic Y identifier is character H (05 hex).

Unit Status

The unit status is recorded in bits 32 to 39 of the CSW. The bits have the following assignments:

Bit	*Designation*
32	Attention (not used)
33	Status modifier (not used)
34	Control unit end (not used)
35	Busy
36	Channel end
37	Device end
38	Unit check
39	Unit exception

Busy (Bit 35)

The busy bit is set if an inline test is running and the subchannel is busy. If a 'start I/O' or 'test I/O' instruction is given, condition code 1 is set in response.

Channel End and Device End (Bits 36 and 37)

Channel end and device end are always set together. They indicate that the line attachment is free to accept another command. If not accompanied by other status bits, the setting of channel end and device end means that the previous command ended normally.

Unit Check (Bit 38)

The unit check bit can be set for several errors or unusual conditions which cause command termination. Unit check is set, for example, if a timeout elapses when no data has been received; when a 'break' signal is received; or if an echo check occurs. For further details of the conditions that can set unit check, see "Sense Information" in this section.

Unit Exception (Bit 39)

The unit exception bit is set when the character sequence FIGS Y (indicating EOT) is received during execution of a 'read' or 'inhibit' command or when a 'write' command attempts to transmit data while characters are being received on the addressed line.

Sense Information

One byte of sense information is available. The bits in sense byte 0 have the following assignments:

Bit	*Designation*
0	Command reject
1	Intervention required
2	Bus out check (not used)
3	Equipment check
4	Data check
5	Overrun
6	Lost data
7	Timeout complete

Command Reject (Bit 0)

The command reject bit is set when an unassigned command, for example, a 'poll' command is given. Command reject is also set when a 'break' command is given when read interruption has not been specified by a 'set line mode' command.

Intervention Required (Bit 1)

Intervention required is set for commands, other than 'enable' or 'set line mode', that are given to a disabled line attachment.

Bus Out Check (Bit 2)

The bus out check bit is not used.

Equipment Check (Bit 3)

The equipment check bit, when set, indicates a hardware error within the line attachment.

Data Check (Bit 4)

The data check bit is set, during execution of a 'read' or

'inhibit' command, when a space level is received instead of a stop bit. This can happen either because of a timing error or because a 'break' signal was received. Data check is also set when an echo check occurs during a write operation.

Overrun (Bit 5)

The overrun bit is set if a character is lost during execution of a 'read' or 'inhibit' command. This can happen when a data transfer to main storage fails.

Lost Data (Bit 6)

The lost data bit is set when characters are lost for reasons other than overrun. Characters are lost if the line receives at least one character before or at the time a 'read' command is accepted; or when a 'halt I/O' or 'halt device' instruction prevents a received character from being transferred to main storage. Lost data cannot be set during execution of a 'prepare' command.

Timeout Complete (Bit 7)

The timeout complete bit is set when 28 seconds have elapsed before the first or any subsequent character has been received during a 'read' command. This occurs also when, during execution of a 'prepare' command, a valid start bit is detected but no stop bit.

BINARY SYNCHRONOUS COMMUNICATION CONTROL

Characteristics

The binary synchronous communication (BSC) line control procedure comprises the command set, the line control characters and sequences required to communicate with any other binary synchronous terminal or processor attachment. This allows telecommunication with other System/360 or System/370 machines provided these are equipped as required.

Line Control Characters

SOH and STX: SOH (start of heading) and STX (start of text) both cause the same action in receive as well as transmit operations: they set the line attachment to text mode. In text mode, block check character accumulation is started and subsequent SOH or STX characters are treated as data (no control function).

ETX and ETB: ETX (end of text) and ETB (end of transmittal block) both cause the same action in transmit and receive modes: they end text mode and the command (unless transparent mode is set). If error index byte mode was specified (by a 'set mode' command), reception of ETX or ETB causes an error index byte to be stored next to ETX or ETB.

ENQ (Inquiry): ENQ ends a 'read' command but has no effect on a 'write' command. When used during a 'poll' command, ENQ causes a line turnaround (a change from transmit to receive mode).

ACK (Positive Acknowledgement): ACK is a sequence consisting of DLE followed by an appropriate character (see description of "DLE" in the following text). ACK ends a 'read' command but has no effect on a 'write' command.

NAK (Negative Acknowledgement): NAK is a single character which ends a 'read' command but has no effect on a 'write' command.

EOT (End of Transmission): EOT ends a 'read' command (if received while the line attachment is not in text mode) but has no effect on a 'write' command.

ITB (Intermediate Text Block): The ITB character does not end a 'read' or 'write' command but resets block check character accumulation, causing the accumulated value to be transmitted (during a 'write' command) or an error index byte to be stored (during a 'read' command if error index byte mode was specified). Transmission or reception then continues with new block check character accumulation.

DLE (Data Link Escape): The DLE character has no function when transmitted or received alone. If specific characters immediately follow DLE, a sequence with control functions is recognized. For example, DLE coupled with 70 (hex) is the ACK-0 reply; DLE coupled with 61 (hex) is the ACK-1 reply; DLE with 7F (hex) is the WABT (wait before transmit) reply. All of these sequences terminate a 'read' command. Other sequences such as DLE/STX set transparent mode. (For details, see the descriptions of individual commands in this section.)

SYN (Synchronization): The SYN character is used ahead of a transmission and is inserted into the message stream after every 56 to 84 characters for the purpose of establishing and maintaining synchronization. Depending on the type of clock (internal or modem clock) either two or seven SYN characters are sent out ahead of a message so that the receiver can synchronize.
Note: For a complete listing of all applicable control characters, see "Appendix A. ICA Code Tables".

Line Transmission Code

The line transmission code used for binary synchronous communication is either EBCDIC or ASCII (ISO*/CCITT** No 5).

Storage byte:	0	1	2	3	4	5	6	7
ASCII relation:	–	7	6	5	4	3	2	1

When ASCII characters are transmitted, the bit position

* International Organization for Standardization.
** Comite'Consultatif International Téléphonique et Télégraphique

shown as a dash (this bit is off while in storage) is replaced by an appropriate parity bit which is transmitted over the line. When ASCII characters are received, the parity bit is stripped off and its bit position is stored as zero. Regardless of the code used, the low-order bit (bit 7 in EBCDIC, bit 1 in ASCII) is always transmitted first. If the data received is coded in ASCII, it is converted to EBCDIC before being transferred to main storage; if the data received is in EBCDIC, it is stored unchanged.

Commands

Figure 86 shows the commands available for binary synchronous communication control.

Hex	Command Code CCW Bits 0 1 2 3 4 5 6 7	Command
02	0 0 0 0 0 0 1 0	Read
01	0 0 0 0 0 0 0 1	Write
06	0 0 0 0 0 1 1 0	Prepare
27	0 0 1 0 0 1 1 1	Enable
2F	0 0 1 0 1 1 1 1	Disable
09	0 0 0 0 1 0 0 1	Poll
1E	0 0 0 1 1 1 1 0	Address prepare
29	0 0 1 0 1 0 0 1	Dial
2B	0 0 1 0 1 0 1 1	Set line mode
23	0 0 1 0 0 0 1 1	Set mode
04	0 0 0 0 0 1 0 0	Sense

Figure 86. BSC Commands [10865]

Read

Whenever the binary synchronous line attachment is enabled and is not executing a write-type command, it monitors the line for activity. Activity is recognized when the steady level on the line (indicating no activity) changes. If changes are sensed, the line attachment decodes the last eight bits received at a specific time. If these eight bits do not represent a SYN character, monitoring continues. If a SYN character is decoded, the next eight bits are gated in and are subsequently checked for their identity with a SYN character. If the second byte thus received is a SYN character, then the line attachment has established character phase, which is a prerequisite for read operations.

When a 'read' command is given, the line attachment may or may not have character phase. If character phase has already been established, execution of the 'read' command progresses. However, if a non-SYN character comes in before the 'read' command is given, the command ends with unit check and the lost data bit is set in the sense byte.

If character phase has not yet been established, the 'read' command causes a three-second timeout to be started. If character phase cannot be established before three seconds have elapsed, the command ends with unit check set and the timeout complete bit is set in the sense byte.

If character phase can be established in time, the line attachment checks whether a control character is received within three seconds after reception of a SYN character. If a control character (other than SYN) cannot be found in time, the command ends with unit check set and the timeout complete bit set in the sense byte.

If character phase can be established and there is no timeout, further actions within the line attachment depend on the data that is actually received, as described in the following text.

1. If ACK, NAK, or ENQ is received, the 'read' command ends with channel end and device end set. The line attachment continues to attempt to establish character phase.
2. If an SOH or STX character is received, the line attachment sets text mode. In text mode, further SOH or STX characters are no longer recognized as control characters, but are treated as text. In addition, the block check character accumulation begins. The SYN characters (which are included in the data stream at 56 to 84 character intervals) are not transferred to main storage but are used to maintain character phase. If characters are received while the line attachment is in text mode, a SYN non-SYN sequence must be received before three seconds have elapsed. This is to prevent a situation in which the line attachment receives text without interspersed synchronization information.

   As text reception continues, each character received updates the block check character accumulation. Being in text mode, the line attachment is sensitive to the following ending characters:

   a. If ETX or ETB is received, the line attachment leaves text mode. Block check character accumulation stops and the attachment awaits the BCC characters from the remote station. Upon reception of these characters (2 bytes), they are compared with the value accumulated locally. Depending on the line code and the checking method used, the block check characters can be two CRC bytes, one LRC byte, or one VRC byte and one LRC byte. If the result is equal, channel end and device end are presented for the 'read' command. If the result shows not equal, unit check is also presented and the data check bit is set in the sense byte. If EIB mode was specified by a 'set mode' or 'set line mode' command, an error index byte is stored next to the ETX or ETB character.

   b. If ENQ is received, the line attachment leaves text mode but does not compare BCC characters. Channel end and device end are presented for the 'read' command.

The foregoing description covers the basic aspects of a 'read' command. There are three variations, however, which alter the behavior of the line attachment during execution of a 'read' command.

1. If an ITB character is received, the attachment stops block check character accumulation, waits for the BCCs from the remote station, and compares these with the accumulated value without ending the read command. Reading continues with the next block for which BCC accumulation is started from an initial value. If the BCC comparison gives an unequal result, data check is set in the sense byte, but this data check is presented to the program only at the end of the read operation.

   If error index byte (EIB) mode was specified by a 'set mode' or 'set line mode' command, reception of an ITB character causes the same BCC comparison but, in addition, an error index byte is stored next to every ITB. This error index byte may contain all zeros or have bit 4 (data check) and/or bit 5 (overrun) turned on, depending on the type of error case. In this manner, each data block will have its own ITB character (and its own error index byte, if EIB mode is in effect). The 'read' command ends when ETX, ETB or EOT is received. If EIB mode was specified, an error index byte is stored next to the ending character. At that time unit check is set in the status (and data check or overrun in the sense byte) if such errors occurred.
2. If transparent text mode was specified via the 'set line mode' command and the DLE/STX sequence is received, the line attachment sets transparent mode. In transparent mode, the attachment is *insensitive* to all control characters; which means that all possible codes (entire ASCII or EBCDIC) are treated as text. However, in transparent mode the attachment is sensitive to the escape sequences which all start with the DLE character. To differentiate between DLE as text data and a DLE-escape sequence, the line attachment examines each DLE and the character that immediately follows it. The action depends on the character that follows DLE. Four actions are possible:
   a. If DLE is followed by another DLE, the first DLE is ignored and the second DLE is transferred to main storage. Transparent reading continues.
   b. If a SYN character follows DLE, the SYN character is ignored. Transparent reading continues. SYN characters which do not follow DLE characters are recognized as data.
   c. If an ITB character follows DLE, the line attachment leaves transparent text mode and continues reading. The BCC is compared and the error index byte is stored (if EIB mode was specified). If thereafter DLE/STX is received again, the line attachment returns to transparent mode.
   d. If an ETB or ETX character follows DLE, the 'read' command ends with channel end and device end set. This terminates transparent text mode. ETB or ETX characters which do not follow a DLE character are treated as data.
3. During execution of a 'read' command, the line attachment may not receive a character that sets text mode (or transparent text mode). When not in text mode, the line attachment is sensitive not only to the control characters that set text mode or end the command but also to all DLE-sequences that consist of DLE followed by any of the characters in column 3 of the ASCII code table (or columns 6 and 7 in the EBCDIC table). Most of these sequences have no particular assignment but some have been agreed upon as a programming convention in IBM support programs (access methods); for example, ACK-0, ACK-1, WABT (wait before transmit), RVI (reverse interruption), DLE/EOT (switched line disconnect signal), and so on. However, all of these assignments concern the program only. For example, ACK-0, ACK-1 are positive acknowledgements with a built-in count that alternates 0, 1, 0, 1 so that the program can discover that an acknowledgement is missing. Reverse interruption is a request from the remote station asking the program to stop transmitting and issue a 'read' command so that a message can be put through. The logical meanings of these DLE sequences are ignored by the line attachment.

The line attachment recognizes any of the DLE column 3 sequences as a signal to terminate the command with channel end and device end. The line attachment remains in receive status and begins to search for character phase.

Write

The 'write' command causes data to be transferred in ascending order of address from the main storage location specified in CCW bits 8 to 31 to the line attachment, for transmission to the remote terminal. When the 'write' command is given, the line attachment stops its continuous search for synchronization unless it is in character phase. If character phase is already established, the 'write' command ends with unit exception. Unit exception in response to a 'write' command indicates that a 'read' command should be issued because of incoming data (some data may already have been lost). If character phase has not been established at the time when a 'write' command is given, the line attachment transmits a pad character. If the clock is in the modem, the pad character is followed by two SYN characters. If the clock is in the line attachment (internal clock), the pad character is followed by seven SYN characters.

The SYN characters are immediately followed by the data from main storage. After every 56 to 84 characters, one SYN character is inserted into the message stream so that the receiving station can correct its clock if necessary. The detailed actions within the line attachment depend on the data transmitted, as described in the following text.

1. If control characters such as ENQ, NAK, or EOT, or character sequences such as ACK-0, ACK-1, WABT, or

RVI are transmitted, no action occurs and the write command does not end. (The receiving station, however, does terminate the corresponding 'read' command.)

2. If the SOH or the STX character is transmitted, the line attachment sets text mode, which means that BCC accumulation is reset and begins again from an initial value. Further SOH or STX characters are not treated as control characters, but as ordinary text data.
3. If an ETX or ETB character is transmitted, the line attachment leaves text mode and transmits the accumulated BCC characters. Channel end and device end are then presented for the 'write' command.

The foregoing text describes a basic 'write' operation. If, however, EIB mode or transparent text mode have been specified, the line attachment is sensitive to certain control characters as follows:

1. If an ITB character is transmitted, the line attachment next transmits the BCC value accumulated up to this point. This value allows the receiving station to compare (and to store the appropriate error index byte if EIB mode has been specified). Execution of the 'write' command continues, beginning with a new BCC accumulation. In ITB mode, a 'write' command ends when ETX or ETB is recognized (same as in non-ITB mode).
2. If the character sequence DLE/STX is transmitted, the line attachment sets transparent text mode if this mode was specified by a 'set line mode' command. Transparent text mode has the following consequences:
   a. Whenever a DLE character is transmitted, the line attachment generates a second DLE which it sends out following the first DLE. This allows the receiving station to differentiate between a DLE control sequence and a DLE character which is treated as data.
   b. If a SYN character is fetched from main storage and transmitted, no action occurs. However, the automatically inserted SYN characters are each preceded by a DLE. This allows the receiving station to differentiate between SYN characters treated as data and SYN characters that are inserted for synchronization purposes only.
   c. If the ending sequence DLE/ETX or DLE/ETB is transmitted, the sequence is not recognized because any DLE is automatically doubled by insertion of another DLE, thus altering the sequence to DLE/DLE ETX or DLE/DLE ETB which has no effect. For this reason, a 'write' command in transparent mode continues until the count in CCW bits 48 to 63 is reduced to zero. Another 'write' command must then be given within three seconds for the explicit purpose of sending just DLE/ETX. The second 'write' command should be chained to the first one to ensure that no other command can be given between them. The line attachment is in the transparent wait state, in which it rejects all commands except 'write' (and 'control no-op'). Since this second 'write' command does not set transparent text mode, the sequence DLE/ETX is not altered by the extra DLE and is therefore understood by the remote station (which is still in transparent receive mode).
   d. If DLE/ITB is to be transmitted, the same situation applies as for DLE/ETX. The sequence DLE/ITB must also be sent via a separate 'write' command which should be chained to its predecessor so that transmission within three seconds is ensured.

Prepare

The 'prepare' command provides a means of alerting the program to the fact that character phase has been obtained at the addressed communication line. Since character phase is a prerequisite for a successful read operation, the 'prepare' command may be chained to a 'read' command (which will then be successful).

When the 'prepare' command is given, the attempts to obtain character phase are monitored. The search for character phase is a continuous process interrupted only by write commands (the search also continues in the absence of any command, provided the line attachment is enabled). If character phase has already been established, channel end and device end are presented in the initial status for the 'prepare' command, otherwise this status is given when character phase is actually obtained. No data transfer occurs and no timeouts are associated with the 'prepare' command.

Enable

The 'enable' command puts the line attachment into the operational state. If the line attachment is not enabled, all commands (except 'enable', 'dial', and 'set line mode') are rejected with unit check set in the CSW and the intervention required bit set in the sense byte. If the 'enable' command is issued to a privately-owned or leased line, channel end and device end are presented when the line attachment detects the 'data set ready' signal being raised by the modem. If 'data set ready' is not detected within one second of the line attachment raising the 'data terminal ready' signal, the 'enable' command ends with unit check set and the intervention required bit is set in the sense byte. If the 'enable' command is given to a switched line, the line attachment is conditioned to answer automatically an incoming call, assuming the modem has auto-answer capability. Channel end and device end are then presented when an incoming call is received. No timeout is associated with the 'enable' command.

Disable

The 'disable' command turns off the addressed line attachment. The disabled line attachment can no longer search for character phase, execute any command (except 'enable', 'dial', or 'set line mode'), or react to an incoming call. If the 'disable' command is given to a private or leased line, channel end and device end are indicated when the 'data set ready' signal from the modem is turned off. If given to a switched line, the command causes the modem to disconnect. A 32-second timeout (for Swedish or UK modems) or a one-second timeout (for all other modems) is started and if the modem has not disconnected before the timeout expires, the 'disable' command ends with unit check set and the timeout complete bit set in the sense byte.

Poll

The 'poll' command provides a means of requesting several remote stations, one after the other, to transmit data to the line attachment. The command is normally used in a multipoint network (where several satellite stations are connected to the same receive line) but it can also be used in a point-to-point installation.

When the 'poll' command is given, the attachment stops its usual search for character phase and transmits the pad character followed by the appropriate number of SYN characters. The SYN characters are followed by data that is fetched from the main storage location specified in CCW bits 8 to 31 and ascending addresses. This data usually consists of a station address and ends with the ENQ character. Up to this point there is no difference between the 'poll' command and a normal 'write' command.

As data is being transmitted, however, the line attachment attempts to detect the ENQ character in the outgoing data stream. When the line attachment detects ENQ, the index character is fetched from storage but not transmitted; it is retained in the line attachment. The line attachment next goes into receive mode *without* ending the 'poll' command. A three-second timeout is started and the search for character phase begins. Further actions by the line attachment depend on the state of the remote station, as described in the following text.

Unsuccessful Poll: If the remote station is inactive, character phase cannot be obtained. The three-second timeout elapses in the line attachment, causing the 'poll' command to end with channel end, device end, and status modifier bits set. If the 'poll' command is chained, the next command is skipped (due to the status modifier being set) and the next sequential command after the skipped command, (which is usually a 'read') is terminated with unit check set and the timeout complete bit set in the sense byte. The index byte (previously fetched) is returned to main storage.

Remote Station Has Nothing to Send: If the remote station is transmitting SYN characters, the line attachment obtains character phase before the timeout elapses. When character phase is obtained, the line attachment checks whether the first non-SYN character received is the EOT character. If the first non-SYN character *is* EOT, the line attachment goes back to transmit mode because the remote station has nothing to send. The next polling data is then fetched from main storage and, when the ENQ character is detected, the line attachment fetches the next index byte and turns around to receive mode, as before.

Successful Poll: If character phase is obtained and the first non-SYN character is *not* EOT, the 'poll' command ends with channel end, device end and status modifier bits set. If chaining is in progress, the status modifier causes the next sequential command to be skipped and the next sequential command after the skipped command is executed. Since this command is usually a 'read', the line attachment then reads in the message from the remote station. Before the first character is transferred to main storage, however, the line attachment returns the index byte (previously fetched) to main storage as an identifier for the message that follows, so that the program knows which remote station has responded.

Note: Polling can also be performed by alternate 'write' and 'read' commands that are chained appropriately.

Address Prepare

The 'address prepare' command allows the program to set up the line attachment to monitor the receive line for its own polling or selection address. This function is required when the line attachment is to operate as a tributary station.

When the 'address prepare' command is given, the line attachment attempts to establish character phase and starts a three-second timeout, unless character phase has already been established. Character phase is required because the line attachment must be able to monitor all communication on the line. Further actions within the line attachment depend on the activity on the receive line, as described in the following text.

1. If the three-second timeout expires, the line attachment enters "adprep monitor mode"* and starts a new three-second timeout. The line attachment remains in adprep monitor mode until it receives the sequence

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* In adprep monitor mode, the line attachment is conditioned to check for an EOT character which is *not* part of text. Such an EOT must be preceded by two SYN characters and followed by a pad character. The pad character serves as a "filler" and ensures that the last bit of the EOT character is safely recognized and that no other character immediately follows the EOT. The EOT must be isolated in this way to be recognized as valid.

SYN, SYN, EOT, pad character. This is a valid EOT sequence and sets the line attachment to "adprep control" mode which is the only state in which it can recognize poll or selection addresses. The 'address prepare' command can be terminated only when a poll or selection address is recognized.

2. If character phase is already established when the 'address prepare' command is given, the line attachment enters adprep monitor mode, starts a three-second timeout and waits for the SYN, SYN, EOT, pad character sequence. When this sequence is received, another three-second timeout is started, because if there is any polling going on, the address should follow EOT before three seconds have elapsed.
3. If character phase is established and a control character such as SOH or STX is received, the line attachment sets adprep monitor mode and text mode but does not transfer data to main storage. Instead, the line attachment monitors the data stream for a valid EOT character. The line attachment is capable of looking for its address only after it has recognized the EOT character because this sets adprep control mode.
4. If character phase is established, EOT has been detected, and one of the tributary station addresses of the line attachment is recognized, further action depends on the type of address received. The line attachment has a selection address and a polling address.
5. If the selection address has been recognized, the 'address prepare' command ends with channel end and device end. This allows chaining to a 'read' command that will read the address into main storage.
6. If the polling address is recognized, the 'address prepare' command ends with channel end, device end and status modifier. This allows chaining to the command after the next sequential command, which should be a 'read' that transfers the polling address to main storage.

Note: When polled, the line attachment is requested to transmit to the remote station (the control station). When selected, the line attachment is requested to receive from the control station.

Dial

The 'dial' command causes the line attachment to be enabled and a data transfer from main storage to the automatic calling unit is performed. If there is no ACU installed, the 'dial' command is rejected and the line attachment is not enabled.

The data is transferred from the location specified in CCW bits 8 to 31 and ascending locations until the count in CCW bits 48 to 63 is reduced to zero. In the data thus transferred, only bits 4 to 7 of each byte are actually placed on the interface (the digit lines) of the calling unit.

The program is responsible for sending only decimal values (0 to 9) as dial information, because the line attachment does not check for decimal validity. The program must also send the correct number of digits, as the line attachment has no provision for detecting an end of number (EON) code.

The dial digits are presented to the ACU at a rate set by the ACU. If the ACU timeout elapses before connection is established, the 'dial' command ends with unit check, and the timeout complete bit is set in the sense byte. If the ACU has its power indicator off, the 'dial' command ends with unit check in the initial status and intervention required is indicated in the sense byte.

Note: The line must be disabled before the 'dial' command is given, otherwise the command is rejected.

Set Line Mode

The 'set line mode' command allows the line attachment to be adjusted to suit the characteristics of the modem, the line, and the remote stations with which it is to operate. When the command is given, up to three bytes of mode-setting information are transferred from main storage to the line attachment. The characteristics which can be specified by each mode-setting byte are described in the following text.

Mode Byte 1: Mode byte 1 allows speed selection. The bit designations and interpretations are shown in the following tables.

Bit	*Designation*
0	(Not used) [0]
1	(Not used) [0]
2	(Not used) [0]
3	Speed select
4	Speed select
5	(Not used) [0]
6	(Not used) [0]
7	(Not used) [0]

Bit 3	*Bit 4*		*Meaning*
0	0	=	1200 bits/sec low (for 2,400/1,200 modem)
0	1	=	1200 bits/sec high (for 1,200/600 modem)
1	0	=	600 bits/sec
1	1	=	(Not used)

A 'set line mode' command with one of the speed selections shown will set the internal clock to the specified speed. The bits marked "not used" must be zero. If there is no internal clock, speed select bit 3 is ignored and speed select bit 4 specifies the lower modem speed when 0, the higher modem speed when 1, unless the modem has only one speed, in which case there will be no action.

Mode Byte 2: Mode byte 2 allows selection of various line and modem properties, as well as special modes. The bits in mode byte 2 have the following meanings assigned:

Bit	*Designation*
0	Continuous request to send
1	Switched network
2	New sync
3	Swedish or UK modem
4	EIB mode
5	Transparent mode
6	ASCII
7	Not used (0)

Continuous Request to Send (Bit 0). When the continuous request to send bit is set, the request to send line to the modem is permanently on as required for duplex operation on a four-wire line. If bit 0 is off, the request to send line is turned on only when a 'write' or 'poll' command is given.

Switched Network (Bit 1) and New Sync (Bit 2). Bits 1 and 2 together can represent several code combinations:

Bit 1	*Bit 2*	
0	0	= Leased line without new sync
0	1	= Leased line with new sync
1	0	= Switched line

New sync is a special method of fast synchronization that allows faster turnaround recovery during polling operations in a multipoint network. New sync is recommended for use with the IBM 3872 Modem, the IBM 3875 Modem, and the Western Electric WE 201 B3 Modem.

Swedish or UK Modem (Bit 3). Swedish and British General Post Office modems use the "connect data set to line" procedure on switched networks and this procedure is employed when bit 3 is set. In addition, a 32-second timeout is used for disconnection. If bit 3 is off, the data terminal ready procedure is used in establishing the line connection and a one-second timeout is used for disconnection.

EIB Mode (Bit 4). When the EIB mode bit is set, an error index byte is generated and stored next to every ITB character that is received. If no ITB character is received, the error index byte is stored next to the ending character (ETX or ETB) of a received message. The error index byte may contain all zeros or may indicate the two types of error that can occur during receive operations. These are data check (unequal BCC compare) which sets bit 4, and overrun (service too late) which sets bit 5.

Transparent Mode (Bit 5). When the transparent mode bit is set, the line attachment becomes sensitive to the DLE sequences that start and stop transparent text mode. This means that any type of information (such as packed decimal data, or program code) can be transmitted or received because all code combinations are treated as text data.

ASCII (Bit 6). When the ASCII bit is set, the line attachment treats all line code received as ASCII, and ASCII is transmitted during write operations. If bit 6 is off, EBCDIC is used.

Note: If no 'set line mode' command is given, the following default values are assumed for mode byte 2:

Not continuous request to send
Leased line
Not new sync
Not Swedish or UK modem
Not transparent mode
EBCDIC.

Mode Byte 3: Mode byte 3 specifies the tributary station address. Any EBCDIC or ASCII character (except SOH, STX, ETX, ETB, EOT, ENQ, DLE, NAK, SYN, or ITB) can be used to specify the address. The address-specifying character is in hexadecimal notation. Bit 2 of mode byte 3 indicates selection if set, polling when off.

The following table shows, as an example, how mode byte 3 would represent station address "B".

Bit	0	1	2	3	4	5	6	7
Binary Value	8	4	2	1	8	4	2	1
Character B = 'C2'	1	1	0	0	0	0	1	0

Bit 2 = 0 indicates polling
= 1 indicates selection

If the same station is addressed, but for selection, the character S (hex E2) must be used (bit 2 set).

Note: It is the responsibility of the operating system to specify the mode in accordance with the actual environment. If, for example, the operating system specifies switched network although a leased line is used, no error indication is given.

Set Mode

The 'set mode' command allows the program to specify whether or not the line attachment is to operate in EIB mode. The command is provided for compatibility reasons because programs written for an IBM 2703 Transmission Control do not use a 'set line mode' command, only a 'set mode' command. If EIB mode is specified, each data block received is provided with an error index that shows whether or not the block was received error-free. When EIB mode is not specified, each block is checked in the same way but there is only a common error indication for the entire record.

One byte is used for specifying EIB mode; the bits have the following meanings assigned:

Bit	*Designation*
0	(Not used)
1	EIB mode (1)
2	(Not used)
3	(Not used)
4	(Not used)
5	(Not used)
6	(Not used)
7	(Not used)

Sense

The 'sense' command causes one byte of sense information to be transferred to the main storage location specified in bits 8 to 31 of the CCW. The contents of the sense byte are described in "Sense Information" in this section.

Unit Status

The unit status is recorded in bits 32 to 39 of the CSW. The bits are assigned as follows:

Bit	*Designation*
32	Attention (not used)
33	Status modifier
34	Control unit end (not used)
35	Busy
36	Channel end
37	Device end
38	Unit check
39	Unit exception.

Status Modifier (Bit 33)

The status modifier bit is set during polling operations in specific cases to allow chaining to the command after the next sequential command. If a 'poll' command has progressed to the point where the polling data has been sent out and the line attachment is in receive mode, the status modifier is set if the first character received after the SYN characters is not the EOT character. If the line attachment operates as a tributary station, the status modifier is set when the polling address (not the selection address) is detected during execution of an 'address prepare' command.

Busy (Bit 35)

The busy bit is set if an inline test is running and the subchannel is busy. If a 'start I/O' or 'test I/O' instruction is given, condition code 1 is set in response.

Channel End and Device End (Bits 36 and 37)

The channel end and device end bits are always presented together when a command has ended (that is, when the subchannel is free). For some commands, the presentation of channel end and device end is in itself an indication that a specific event has occurred. For example, when channel end and device end are presented for the 'prepare' command, this indicates that character phase has been established. For an 'address prepare' command, this status indicates that the selection address has been detected.

Unit Check (Bit 38)

Unit check is a summary indication which can be set by several different errors or unusual conditions. For example, if a disabled line attachment is addressed or if a timeout has elapsed, unit check is set. For more detailed information on the conditions which set unit check, see "Sense Information" in this section.

Unit Exception (Bit 39)

The unit exception bit is set when certain specific conditions occur during the execution of a command. These conditions, which are described in the following list, are unique for each command.

1. If a 'write' command is given when character phase is already being established, unit exception is set because a transmission from the remote station has started or is in progress. The 'write' command is not executed but is terminated immediately. The same applies to the 'poll' command under the same circumstances.
2. If the EOT character is recognized during execution of a 'read' command, the command is terminated with unit exception set.
3. For all other commands, unit exception is set whenever such commands are terminated by 'halt I/O' or 'halt device' instructions before any action could occur.

Sense Information

One byte of sense information is available, which can be transferred to main storage via a 'sense' command. A 'sense' command should be given whenever unit check is indicated. The bits in sense byte 0 have the following meanings assigned:

Bit	*Designation*
0	Command reject
1	Intervention required
2	Bus out check (not used)
3	Equipment check
4	Data check
5	Overrun
6	Lost data
7	Timeout complete

Command Reject (Bit 0)

The command reject bit is set during command initiation if an invalid command is given to a line attachment or if the line is in a condition in which the command cannot be executed. The command is terminated immediately with only unit check set in the CSW. The following conditions cause command rejection:

1. Bit positions 2 to 7 of the command code in the CCW do not match bit positions 2 to 7 of any of the valid commands.
2. A 'break' or 'inhibit' command is given to a synchronous line.
3. A 'read', 'autopoll', 'write', 'address prepare', or 'prepare' command is given to a synchronous line that has not been enabled.
4. A command other than a 'write', 'sense' or 'control no-op' has been given to a synchronous line while in the transparent wait condition (transparency feature must be installed).
5. A 'dial' command is given but no ACU is installed.
6. The 'data terminal ready' signal is detected when a 'dial' command is initiated (that is, the addressed line is not in the disabled state when the 'dial' command is initiated).

Intervention Required (Bit 1)

The intervention required bit, when set, normally causes immediate termination of the current command, and channel end, device end, and unit check are set in the CSW when stored at I/O interruption. The following conditions cause intervention required to be set:

1. The 'data set ready' signal is inactive at command initiation of a 'read', 'prepare', 'address prepare', 'write' or 'autopoll' command.
2. The 'data set ready' signal is inactive during execution of a 'read', 'prepare', 'address prepare' or 'autopoll' command.
3. An 'enable' command is given to an already enabled line ('data terminal ready' signal active), but the 'data set ready' signal is not active.
4. The 'clear to send' signal has not been activated by the modem before the three-second timeout ends during 'write' command initiation, 'autopoll' command initiation, or an autopoll read to autopoll write turnaround.
5. The 'clear to send' signal is inactive during execution of a 'write' command or (in the autopoll write state) during execution of an 'autopoll' command.
6. In two-wire operations (not continuous request to send), the 'clear to send' signal is not de-activated by the modem before the one-second timeout elapses either at 'write' command termination or at 'autopoll' write-to-read turnaround.
7. A character underrun condition is detected during a 'write' command or an 'autopoll' command in the autopoll write state. Intervention required is set together with the overrun bit. The command continues to its normal end.
8. In modem-clocked operation, a clock check has been presented (while the 'data set ready' signal was still present) during the execution of a 'write' command or 'autopoll' command in the autopoll write state.
9. The ACU's power indicator signal was inactive at 'dial' command initiation or has become inactive during execution of a 'dial' command.
10. The 'data line occupied' signal is active when a 'dial' command is initiated.
11. The 'data set ready' signal is not activated by the modem within one second after the 'data terminal ready' signal was presented to the modem during execution of an 'enable' command on a leased line configuration.
12. The ACU does not indicate either 'present next digit' or 'abandon call and retry' within three seconds after 'data terminal ready' and 'call request' were presented to the ACU during the execution of a 'dial' command.
13. The ACU fails to indicate either 'not present next digit' or 'abandon call and retry' within three seconds after 'digit present' was presented to the ACU during execution of a 'dial' command.
14. The ACU does not present either 'data set ready' or 'abandon call and retry' within 96 seconds after all dialing digits and the 'not digit present' signal have been presented to the ACU during execution of a 'dial' command.

Equipment Check (Bit 3)

The equipment check bit is set if an ICA hardware check is detected. Such checks occur in the internal microprogram that controls the line attachment. Equipment check causes immediate termination of the current command. Channel end, device end, and unit check are set in the CSW.

Data Check (Bit 4)

The data check bit is only set during execution of a 'read' command. It is set in the following situations:

1. A BCC noncompare is detected during execution of a 'read' command. If this happens, the command is allowed to continue to its normal end.
2. The line has ASCII code specified and a VRC error (even parity) is detected during execution of a 'read' command. If this happens, the command is allowed to continue to its normal end.

Overrun (Bit 5)

The setting of the overrun bit does not cause the command to terminate immediately but allows it to continue to its normal end. The overrun bit is set in the following situations:

1. An overrun condition is detected during execution of a 'read', 'prepare' or 'address prepare' command or during execution of an 'autopoll' command while the line attachment is in the receive state.
2. An underrun condition is detected during execution of a 'write' command or during execution of an 'autopoll' command while the line attachment is in the transmit state. If this occurs, intervention required is set together with the overrun bit.

Lost Data (Bit 6)

The lost data bit is set in the following situations:

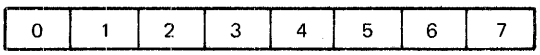
1. The data-lost flag bit is detected during command initiation, indicating that at least one full character was received and lost before the command was given. The command is allowed to continue to its normal end.
2. The length count has been reduced to zero but data is still coming in during execution of a 'read' command. The command is terminated immediately.
3. The line attachment is executing a 'read' command when a 'halt I/O' instruction is given, causing the command to be terminated.
4. The 'data set ready' or 'present next digit' signal is active during command initiation for the 'dial' command, or 'data set ready' rises before the dial-end sequence has been set during execution of the 'dial' command. In either case the command is terminated immediately.

Timeout Complete (Bit 7)

When the timeout complete bit is set, the command in progress is terminated immediately. Timeout complete is set in the following situations:

1. The line attachment is executing a 'read' command and does not receive any control character (except SYN) within three seconds of the beginning of the 'read' command.
2. The line attachment is executing a 'read' command and has not received a SYN character followed by a non-SYN character within three seconds of the previous SYN non-SYN while in text mode, or (with the transparency feature installed) has not received DLE, SYN, non-DLE within three seconds from the previous DLE, SYN, non-DLE while in transparent text mode.
3. The line has the transparency feature specified in the 'set line mode' command and a second 'write' command is issued later than three seconds after the termination of a 'write' command that placed the adapter in transparent mode. This second 'write' ends immediately with the timout complete bit set.
4. The 'abandon call and retry' signal of the ACU has become active during initiation or execution of a 'dial' command.
5. The line attachment is operating as control station on a data link and has been executing a 'poll' command. After the transmission of an autopoll sequence to a tributary station the control station (in the autopoll receive state) waits for three seconds for an answer from the tributary station. If no answer has been received within three seconds, the 'poll' command is ended and chained to a 'read' command. During the initiation of the 'read' command, the index byte is transferred to main storage and the 'read' command is then immediately ended with the timeout complete bit set in the sense byte.
6. The 'data set ready' signal is not de-activated by the modem within one second (not Swedish or UK modem) or 32 seconds (Swedish or UK modem) after the 'data terminal ready' signal has been dropped, during the execution of a 'disable' command.

		Lower case								Upper case							
		Main Storage Byte Positions 0, 1, 2, 3, (S, B, A, 8)															
Byte Positions		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
4, 5, 6, 7 (4, 2, 1, C)	Hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0		8	@		Ⓝ —			h		*	¢		Ⓝ —			H
0001	1	Space			y		q	&		Space			Y		Q	+	
0010	2	1			z		r	a		=			Z		R	A	
0011	3		9	/		j			i		(	?		J			I
0100	4	2					Minus Zero (MZ)	b		<						B	
0101	5		0	s		k			Plus Zero (PZ)		)	S		K			
0110	6		Ⓓ EOA #	t		l			Ⓨ		Ⓓ "EOA	T		L			Ⓨ ¬
0111	7	3			,		$	c					I		!	C	
1000	8	4			Bypass		Re-store	d		:			Bypass		Re-store	D	
1001	9		Punch On (PN)	u		m			Punch Off (PF)		Punch On (PN)	U		M			Punch Off (PF)
1010	A		Reader Stop (RS)	v		n			Horiz Tab		Reader Stop (RS)	V		N			Horiz Tab
1011	B	5			LF		CR / LF	e		%			LF		CR / LF	E	
1100	C		Up-shift	w		O			Down-shift		Up-shift	W		O			Down-shift
1101	D	6			Ⓑ EOB		Back-space	f		–			Ⓑ EOB		Back-space	F	
1110	E	7			Prefix		Idle	g		>			Prefix		Idle	G	
1111	F		Ⓒ EOT	x		p			Delete		Ⓒ EOT	X		P			Delete



= These codes perform no function in the 1050 Data Communication System but are valid data codes. They are not printable.

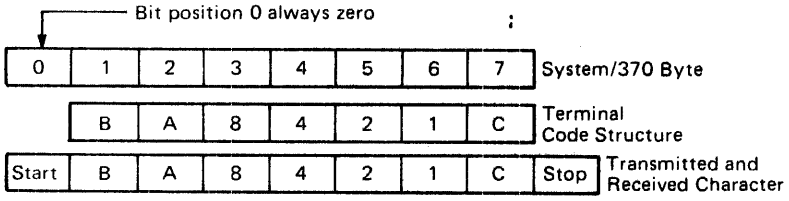
= Duplicate Assignment

Notes:

1. *Equivalent Functions*
   CR/LF = NL LF = Index
2. *S-bit* position (0 for lower case, set for upper case) inserted on receive operations or deleted on transmit operations. Insertion/deletion performed by equipment.
3. *Start and stop bits* are deleted at the ICA during receive operations, added at the ICA during transmit operations.

Figure 87. Code Structure for 1050 Data Communication System in IBM Terminal Control – Type 1 Operations [10866]

		Main Storage Byte Positions 0, 1, 2, 3, (0, B, A, 8)							
Byte Positions		0000	0001	0010	0011	0100	0101	0110	0111
4, 5, 6, 7 (4, 2, 1, C)	Hex	0	1	2	3	4	5	6	7
0000	0		8	Add		Ⓝ			H
0001	1	Space			Y		Q	+	
0010	2	1			Z		R	A	
0011	3		9	/		J			I
0100	4	2			.		Mes-sage	B	
0101	5		0	S		K	*		Re-store
0110	6		Ⓓ EOA #	T		L		:	Ⓨ
0111	7	3					$	C	
1000	8	4					*	D	
1001	9			U		M		!	Subtr
1010	A			V		N			Tab
1011	B	5			LF		CR	E	
1100	C			W		O			
1101	D	6			Ⓑ EOB	;		F	
1110	E	7					Idle	G	
1111	F		Ⓒ EOT	X		P			Delete



Note: Start and stop bits are deleted at the ICA during receive operations, added at the ICA during transmit operations.

Figure 88. Code Structure for 1060 Data Communication System in IBM Terminal Control – Type 1 Operations [10867]

		Lower case								Upper case							
		Main Storage Byte Positions 0, 1, 2, 3, (S, B, A, 8)															
Byte Positions		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
4, 5, 6, 7 (4, 2, 1, C)	Hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0		8	@		— ⓝ			h		°	¢		— ⓝ			H
0001	1	Space			y		q	&		Space			Y		Q	+	
0010	2	1			z		r	a		∓			Z		R	A	
0011	3		9	/		j			i		(	?		J		.	I
0100	4	2						b		< o						B	
0101	5		0	s		k					)	S		K			
0110	6		Ⓓ EOA #	t		l			Ⓨ •		" ± Ⓓ	T		L			ⓨ
0111	7	3			Ⓢ		$	c		;			!		!	C	
1000	8	4						d		:						D	
1001	9			u		m						U		M			
1010	A			v		n			Horiz Tab			V		N			Horiz Tab
1011	B	5			LF (Notes 3 & 5)		NL	e		%			LF (Notes 3 & 5)		NL	E	
1100	C		Up-shift	w		o			Down-shift		Up-shift	W		O			Down-shift
1101	D	6			Ⓑ EOB		Back-space	f		,			Ⓑ EOB		Back-space	F	
1110	E	7					IDLE	g		> "					IDLE	G	
1111	F		Ⓒ EOT	x		p						X		P			

0	1	2	3	4	5	6	7	System/370 Byte
S	B	A	8	4	2	1	C	Terminal Code Structure
Start	B	A	8	4	2	1	C	Stop — Transmitted and Received Character

= PTTC/EBCDIC characters are shown above dashed line. PTTC/BCD characters are shown below dashed line.

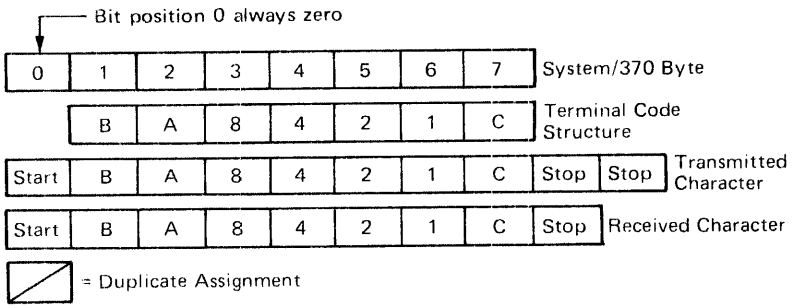
= Characters in undashed boxes are common to PTTC/BCD and PTTC/EBCDIC

Notes:

1. Start and stop bits are deleted at the ICA during receive operations, added at the ICA during transmit operations.
2. S-bit position (0 for lower case, set for upper case) is inserted during receive operations, deleted during transmit operations. Insertion/deletion is performed by equipment.
3. LF (line feed) performs the indexing function.
4. NL (new line) performs the carrier return and line feed function.
5. The following characters (not used by 2740 or 2741 Communication Terminals) are provided for PTTC/BCD and PTTC/EBCDIC programming considerations with the 1050 Data Communication System:
   - Punch ON (PN) '09' and '99'
   - Bypass (BY) '38' and 'B8'
   - Restore (RES) '58' and 'D8'
   - Punch OFF (PF) '79' and 'F9'
   - Delete (DEL) '7F' and 'FF'
   - Prefix (PRE) '3E' and 'BE'.
6. In the 2741, the index key is replaced by an attention key: no indexing functions can be performed during transmission. The indexing function *is* performed when the terminal receives an index character from the line.

Figure 89. Code Structure for 2740 Communication Terminal or 2741 Communication Terminal in IBM Terminal Control – Type 1 Operations [10868]

Byte Positions		Main Storage Byte Positions 0, 1, 2, 3, (0, B, A, 8)							
		0000	0001	0010	0011	0100	0101	0110	0111
4, 5, 6, 7 (4, 2, 1, C)	Hex	0	1	2	3	4	5	6	7
0000	0		8	@ 0 (see Note)		Ⓝ			H
0001	1	Space			Y		Q		
0010	2	1			Z		R	A	
0011	3		9	/		J			I
0100	4	2						B	
0101	5		0 (see Note)	S		K			.
0110	6		Ⓓ EOA	T		L			Ⓨ EOFC
0111	7	3			Ⓢ		$	C	
1000	8	4						D	
1001	9			U		M			
1010	A			V		N			Horiz. Tab
1011	B	5			LF		LF/CR	E	
1100	C			W		O			
1101	D	6			Ⓑ EOB			F	
1110	E	7						G	
1111	F		Ⓒ EOT	X		P			EOC Delete

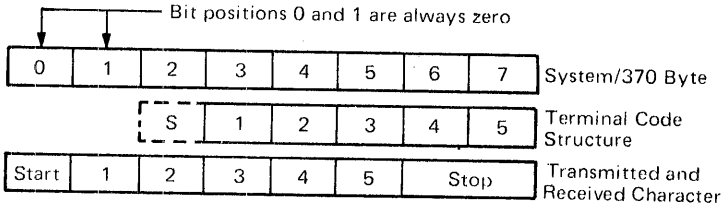


Notes:

1. The 1031 transmits the numeric zero as an A-bit only. The 1033 receives the numeric zero as a C-8-2 code and @ as an A-bit only code.
2. Pad Characters = Hex DF = 11011111.
3. Start and stop bits are deleted at the ICA during receive operations, added during transmit operations.
4. EOFC = end of first card.

Figure 90. Code Structure for 1030 Data Collection System in IBM Terminal Control – Type 2 Operations [10869]

		Main Storage Byte Positions 0, 1, 2, 3 (0, 0, S, 1)			
Byte Positions		0000	0001	0010	0011
4, 5, 6, 7 (2, 3, 4, 5)	Hex	0	1	2	3
0000	0	Blank	E	Blank	3
0001	1	T	Z	5	"
0010	2	CR	D	CR	$
0011	3	O	B	9	5/8
0100	4	Space	S	Space	Bell
0101	5	H	Y	◆	6
0110	6	N	F	7/8	1/4
0111	7	M	X	•	/
1000	8	LF	A	LF	–
1001	9	L	W	3/4	2
1010	A	R	J	4	,
1011	B	G	FIGS↑	&	FIGS↑
1100	C	I	U	8	7
1101	D	P	Q	0	1
1110	E	C	K	1/8	1/2
1111	F	V	LTRS↓	3/8	LTRS↓

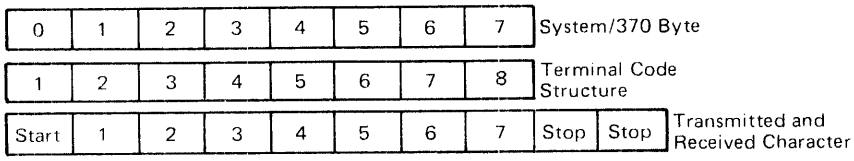


Notes:

1. S-bit position (0 for lower case [LTRS], set for upper case [FIGS]) is inserted during receive operations, deleted during transmit operations. Insertion/deletion is performed by equipment.
2. ↑ = upshift character
   ↓ = downshift character

Figure 91. Code Structure for A T & T 83 B2/83 B3 Terminals and Western Union Plan 115A Terminals in Telegraph Terminal Control – Type 1 Operations [10870]

		Main Storage Byte Positions 0, 1, 2, 3, (1, 2, 3, 4)															
Byte Positions		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
4, 5, 6, 7 (5, 6, 7, 8)	Hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	Null			Form Feed		Line Feed				Horiz Tab	WRU		EOM			Shift In
0001	1	Null		EOT	Form Feed	EOA	Line Feed		Shift Out	SOM	Horiz Tab	WRU	Return	EOM	Vert-ical Tab	Bell	Shift In
0010	2		H	D		B			N	A			M		K	G	
0011	3	@	H	D	L	B	J	F	N	A	I	E	M	C	K	G	Q
0100	4		(	$		"			.	!			–		+	,	
0101	5	SP	(	$		"	*	&	.	!	)	%	–	#	+	,	/
0110	6																
0111	7																
1000	8																
1001	9																
1010	A	P			\		Z				Y	U		S			←
1011	B	P	X	T		R	Z	V	↑	Q	Y	U	]	S	[	W	←
1100	C	O			<		:				9	5		3			?
1101	D	O	8	4	<	2	:	6	>	1	9	5	=	3	;	7	?
1110	E																
1111	F																Delete



Notes:

1. When two codes are shown for a single character, the shaded indication denotes the bit configuration due to the parity bit being held in Mark Hold state. The companion bit configuration has even parity.
2. Start/stop bits are deleted at the ICA during receive operations, added at the ICA during transmit operations.

Figure 92. Eight-Level TWX Code for Standard Keyboard Arrangement in Telegraph Terminal Control – Type 2 Operations [10871]

		Main Storage Byte Positions 0, 1, 2, 3 (0, 1, 2, 3)															
Byte Positions		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
4, 5, 6, 7 (4, 5, 6, 7)	Hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	NUL	DLE	DS		SP	&	–									0
0001	1	SOH	DC1	SOS				/		a	j			A	J		1
0010	2	STX	DC2	FS	SYN					b	k	s		B	K	S	2
0011	3	ETX	DC3							c	l	t		C	L	T	3
0100	4	PF	RES	BYP	PN					d	m	u		D	M	U	4
0101	5	HT	NL	LF	RS					e	n	v		E	N	V	5
0110	6	LC	BS	EOB / ETB	UC					f	o	w		F	O	W	6
0111	7	DEL	IL	PRE / ESC	EOT					g	p	x		G	P	X	7
1000	8		CAN							h	q	y		H	Q	Y	8
1001	9		EM							i	r	z		I	R	Z	9
1010	A	SMM	CC	SM		¢	!										
1011	B	VT					$	,	≠								
1100	C	FF	IFS		DC4	<	*	%	@								
1101	D	CR	IGS	ENQ	NAK	(	)	_	'								
1110	E	SO	IRS	ACK		+	;	>	=								
1111	F	SI	IUS	BEL	SUB	|	¬	?	"								

0	1	2	3	4	5	6	7	System/370 Byte
0	1	2	3	4	5	6	7	EBCDIC Structure
0	1	2	3	4	5	6	7	Transmitted and Received Character

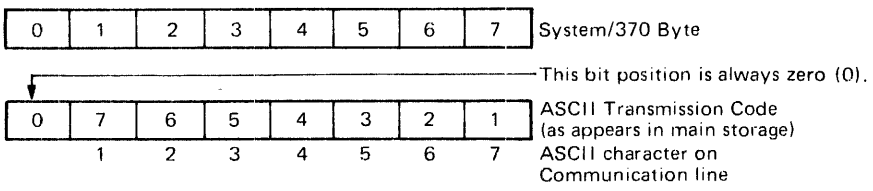
= Duplicate Assignment

Notes:

1. During receive operations in non-text mode, the DLE character, followed by any of the bit configurations in columns 6 or 7, will cause the command to be ended. However, only those bit configurations indicated by ▨ are valid.
2. The following DLE sequences are defined.
   '70' - ACK0
   '61' = ACK1
   '7F'= WABT

Figure 93. EBCDIC, as Used for Binary Synchronous Communication Control [10872]

		Main Storage Byte Positions 0, 1, 2, 3 (0, 7, 6, 5)															
Byte Positions		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
4, 5, 6, 7 (4, 3, 2, 1)	Hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	NUL	DLE	SP	0	@	P	\	p								
0001	1	SOH	DC1	!	1	A	Q	a	q								
0010	2	STX	DC2	"	2	B	R	b	r								
0011	3	ETX	DC3	#	3	C	S	c	s								
0100	4	EOT	DC4	$	4	D	T	d	t								
0101	5	ENQ	NAK	%	5	E	U	e	u								
0110	6	ACK	SYN	&	6	F	V	f	v								
0111	7	BEL	ETB	'	7	G	W	g	w								
1000	8	BS	CAN	(	8	H	X	h	x								
1001	9	HT	EM	)	9	I	Y	i	y								
1010	A	LF	SUB	*	:	J	Z	j	z								
1011	B	VT	ESC	+	;	K	[	k	{								
1100	C	FF	FS	,	<	L	\	l	¦								
1101	D	CR	GS	-	=	M	]	m	}								
1110	E	SO	RS	.	>	N	^	n	~								
1111	F	SI	US	/	?	O	_	o	DEL								



Notes:

1. During receive operations in non-text mode, the DLE character, followed by any character appearing in column 3, causes the command to be ended.
2. There are three DLE sequences:
   '30' = ACK0
   '31' = ACK1
   '3F' = WABT

Figure 94. ASCII, as Used for Binary Synchronous Communication Control [10873]

Appendix B. Instruction Timings

The instruction timings listed in the following tables are for a 3115 with its location 80 timer enabled. To allow for the slight performance degradation caused by updating of the location 80 timer, the tables assume that a microinstruction is executed in 450.22 ns; the actual execution time is 450.0 ns. When the location 80 timer is disabled, CPU performance improves by 0.18%.

If program event recording is enabled, the execution time of a microinstruction is increased by a certain time, the exact value of which depends on the class of events recorded, as follows:

74.65 μs increase for successful branch instruction
96.80 μs increase for instruction fetching
73.7 μs increase for storage alteration
72.8 μs increase for general register alteration
102.3 μs increase if all four of the above classes are to be recorded.

Note: These figures do not include the time taken by the PER program interruption.

If address compare mode is specified for instruction fetching, the execution time of a microinstruction increases by 35.3 μs.

The timing formulas in the tables are correct for processing with dynamic address translation when the logical addresses are contained in the translation lookaside buffer (TLB). If the required address is not in the TLB, translation takes an extra 148 μs. When the tables give separate times for DAT mode (as in the BALR instruction), these timings are based on a 2K page size.

Timings shown in the tables for floating-point instructions assume no pre- or post-normalization.

Parameters for Instruction Timing Formulas

Symbol	Definition
CC0	1 if condition code 0; otherwise 0.
CC3	1 if condition code 3; otherwise 0.
C_{DD}	1 if dividend is negative; otherwise 0.
C_{DR}	1 if divisor is negative; otherwise 0.
C_{MD}	1 if multiplicand is negative; otherwise 0.
C_{MR}	1 if multiplier is negative; otherwise 0.
C_{RE}	1 if result (quotient) is negative; otherwise 0.
D	Number of digit selectors or significant starters in the first operand.
E	Number of equal bytes, left-to-right.
F	Number of field separators in the first operand.
log (RES)	$_{10}$ log of decimal result.
M	Number of message characters in the first operand.
N	Total number of bytes in the first operand (instructions with a single length field).
N_1	Total number of bytes in the first operand.
N_2	Total number of bytes in the second operand.
N_B	Number of 1-bits in the absolute form of the multiplier (for floating point fraction only).
nbm	Number of complete blocks of 256 bytes moved or compared.
nbp	Number of complete blocks of 256 bytes padded.
nc	Number of bytes compared in main storage.
NMD	Decimal sum of all digits of multiplier.
nm3	Number of 1-bits in mask M3.
np	Number of bytes compared against padding character.
NQ	Number of 1-bits in the absolute form of the quotient.
NQD	Decimal sum of all digits of quotient.
nrb	Number of residual bytes moved or compared.
nrp	Number of residual bytes padded.
nr1	Number of times general register 1 is set.
nz	Number of bytes in the absolute form of the multiplier, which are zero (for floating point fraction only).
n/z	Number of bytes containing leading zeros.
ODD	1 if operand starts on odd boundary, otherwise 0.
R	Number of registers invoked.
RC	1 if absolute value of second operand exceeds first operand; otherwise 0 (recomplement).
R_T	IOP response time.
S	0 if base register specified; 1.35 if no base register specified.
s	Number of signs in the second operand.
S_1	0 if base register used; 0.45 μs if unused.
S_2	0 if base register used; −0.9 μs if unused.
T	0 if base addressing; 0.45 if B_1 is 0; 1.35 if B_2 is 0; 1.80 if B_1 and B_2 are 0.
μ	0 if all function bytes are zero; 1 if a non-zero function byte is found.
X_1	0 if single indexing; −0.45 if no indexing; +1.8 if double indexing.
X_2	0 if indexing with base register; −0.9 if no indexing; +0.45 if indexing with X-register; +1.8 if double indexing.

Instruction	Format	Op Code	Mnemonic	Average Time in Microseconds	Notes
Add	RR	1A	AR	8.14 – 0.45CC0 + 0.45CC3	
Add	RX	5A	A	14.47 + X_1 – 0.45CC0 + 0.45CC3	+ 0.9 – ODD
Add decimal	SS	FA	AP	81.83 + 5.43N_1 + 3.17N_2	– 0.45 if B_1 is 0; – 1.35 if B_2 is 0
				85.92 + 5.43N_1 + 3.17N_2 + RC x 2.26N_1	
Add halfword	RX	4A	AH	14.47 + X_1 – 0.45CC0 £ 0.45CC3	+ 0.45ODD
Add logical	RR	1E	ALR	7.69	
Add logical	RX	5E	AL	14.02 + X_1	+ 0.9ODD
Add normalized (long)	RR	2A	ADR	57.47	
Add normalized (long)	RX	6A	AD	64.77	+ 1.8ODD
Add normalized (short)	RR	3A	AER	46.49	
Add normalized (short)	RX	7A	AE	51.61 + X_1	+ 0.9ODD
Add unnormalized (long)	RR	2E	AWR	43.41	
Add unnormalized (long)	RX	6E	AW	66.91 + X_1	+ 1.8ODD
Add unnormalized (short)	RR	3E	AUR	39.80	
Add unnormalized (short)	RX	7E	AU	50.19 + X_1	+ 1.8ODD
AND	RR	14	NR	7.24 – 1.35CC0	
AND	RX	54	N	12.66 + X_1 + 1.35CC0	
AND	SI	94	NI	10.85 – S_1	
AND	SS	D4	NC	24.40 – T + 4.52N	
Branch and link	RR	05	BALR	12.21	
				16.28	
				19.44	
				20.35	
				15.83	
				19.44	
Branch and link	RX	45	BAL	18.54 + X_2	
				24.87 + X_2	
				17.19 + X_2	
Branch on condition	RR	07	BCR	4.07	
				6.33	
Branch on condition	RX	47	BC	4.52	
				8.14 + X_1	
Branch on count	RR	06	BCTR	7.24	
				9.95	
Branch on count	RX	46	BCT	9.50	
				11.31 + X_2	
Branch on index high	RS	86	BXH	18.54	
				17.18	+ 2.70 if R3 is even
Branch on index low or equal	RS	87	BXLE	See BXH	
Compare	RR	19	CR	12.21 – 0.45CC0	Equal signs of operands
				5.42	Unequal signs of operands
Compare	RX	59	C	17.18 + X_1 – 0.45CC0	Equal signs of operands
				11.31 + X_1	Unequal signs of operands + 0.9ODD
Compare decimal	SS	F9	CP	67.85 – T + 4.97N_1 + 3.17 N_2	
Compare halfword	RX	49	CH	16.73 + X_1 – 0.45CC0	
Compare logical	RR	15	CLR	10.85 – 0.45CC0	
Compare logical	RX	55	CL	16.73 + X_1 – 0.45CC0	
Compare logical	SI	95	CLI	11.31 – S_1 – 0.45CC0	
Compare logical	SS	D5	CLC	24.87 – T + 4.07E – 0.45CC0	
Compare logical character under mask	RS	BD	CLM	9.95 – S_1	
				18.54 – S_1 + 0.90nm3 – 0.45CC0	
Compare logical (long)	RR	0F	CLCL	33.01 + 4.07nc + 2.26np	
Compare (long)	RR	29	CDR	46.13	
Compare (long)	RX	69	CD	49.23 + X_1	+ 1.8ODD

Instruction	Format	Op Code	Mnemonic	Average Time in Microseconds	Notes
Compare (short)	RR	39	CER	35.73	
Compare (short)	RX	79	CE	$37.82 + X_1$	+0.9ODD
Convert to binary	RX	4F	CVB	$214.81 + X_1 - 23.97nlz$	+1.8ODD
Convert to decimal	RX	4E	CVD	$44.32 + X_1 + 36.63\log(RES)$	+3.6ODD
Divide	RR	1D	DR	$205.74 - 4.97C_{DR} + 12.21C_{DD} + 4.07C_{RE} + 2.26NQ$ $116.22 - 4.97C_{DR} + 12.21C_{DD} + 4.07C_{RE} + 2.26NQ$	
Divide	RX	5D	D	$210.26 + X_1 - 4.97C_{DR} + 12.21C_{DD} + 4.07C_{RE} + 2.26NQ$ $120.31 + X_1 - 4.97C_{DR} + 12.21C_{DD} + 4.07C_{RE} + 2.26NQ$	+0.9ODD
Divide decimal	SS	FD	DP	$287.53 - T + 78.76N_2 + 22.61N_{QD}$	
Divide (long)	RR	2D	DDR	600.52; 815.28	
Divide (long)	RX	6D	DD	606.61; 821.05	−1.8ODD
Divide (short)	RR	3D	DER	203.97; 248.29	
Divide (short)	RX	7D	DE	210.07; 252.97	−0.9ODD
Edit	SS	DE	ED	$26.23 - T + 9.95D + 7.69F + 3.62s + 5.88M$ $32.55 - T + 13.57D + 10.85F + 3.62s + 9.04M$	
Edit and mark	SS	DF	EDMK	$26.68 - T + 9.95D + 7.69F + 3.62s + 5.88M + 4.07nr1$ $33.00 - T + 13.57D + 10.85F + 3.62s + 9.04M$	
Exclusive OR	RR	17	XR	$6.78 + 1.35CC0$	
Exclusive OR	RX	57	X	$12.66 + X_1 + 1.35CC0$	
Exclusive OR	SI	97	XI	$10.85 - S_1$	
Exclusive OR	SS	D7	XC	$24.85 - T + 4.52N$	
Execute	RX	44	EX	$59.25 + X_2$ (not DAT) $63.32 + X_2$ (DAT)	+1.35 if R1 is not zero −4.07 if subject is successful branch
Halt device	SI	9E	HDV	$38.80 - S_2 + R_T$ $43.41 - S_2$	
Halt I/O	SI	9E	HIO	$38.80 - S_2 + R_T$	
Halve (long)	RR	24	HDR	34.32	
Halve (short)	RR	34	HER	28.91	
Insert character	RX	43	IC	$10.40 + X_1$	
Insert characters under mask	RS	BF	ICM	$10.40 - S_1$ $14.47 - S_1 + 1.80nm_3$	
Insert storage key	RR	09	ISK	17.63	−0.45 if EC mode
Load	RR	18	LR	5.87	
Load	RX	58	L	$11.31 + X_1$	+0.9ODD
Load address	RX	41	LA	$9.04 + X_2$	
Load and test	RR	12	LTR	$7.23 + 0.45CC0$	
Load and test (long)	RR	22	LTDR	20.35	
Load and test (short)	RR	32	LTER	16.28	
Load complement	RR	13	LCR	$12.21 - 0.45CC0 + 0.9CC3$	
Load complement (long)	RR	23	LCDR	20.80	
Load complement (short)	RR	33	LCER	16.73	
Load control	RS	B7	LCTL	$52.39 - S_2 + 10.85R$ (BC) $55.36 - S_2 + 10.85R$	
Load halfword	RX	48	LH	$11.31 + X_1$	+0.45ODD

Instruction	Format	Op Code	Mnemonic	Average Time in Microseconds	Notes
Load (long)	RR	28	LDR	16.73	
Load (long)	RX	68	LD	20.56	+ 1.80DD
Load multiple	RS	98	LM	9.04 − S_1 + 2.71R	
Load negative	RR	11	LNR	11.31	− 4.53 if R_2 is negative
Load negative (long)	RR	21	LNDR	20.80	
Load negative (short)	RR	31	LNER	16.73	
Load positive	RR	10	LPR	12.66	− 4.07 if CC0; + 0.9 if CC3; − 4.97 if R2 positive
Load positive (long)	RR	20	LPDR	20.80	
Load positive (short)	RR	30	LPER	16.73	
Load PSW	RS	82	LPSW	64.02 − S (BC) 67.13 − S (EC without DAT) 75.27 − S (EC with DAT)	
Load Real Address	RX	B1	LRA	119.85	
Load (short)	RR	38	LER	13.11	
Load (short)	RX	78	LE	16.85 + X_1	+ 0.90DD
Monitor call	SI	AF	MC	13.57 − S_2 107.67 − S_2 113.03 − S_2 126.60 − S_2	
Move	SI	92	MVI	9.95 − S_1	
Move	SS	D2	MVC	23.96 − T + 1.35N	
Move (long)	RR	0E	MVCL	28.94 51.56 + 354.49nbm + 1.35nrb 62.86 + 354.49nbm + 1.35nrb + 0.90nrp + 177.20nbp	
Move numerics	SS	D1	MVN	23.51 − T + 4.52N	
Move with offset	SS	F1	MVO	29.39 − T + 4.52N_1 + 0.90N_2	
Move zones	SS	D3	MVZ	28.03 − T + 4.52N	
Multiply	RR	1C	MR	192.16 + 4.52C_{MV} + 4.52C_{MD} + 8.14C_{RE} − 36.18nz + 2.26N_B	
Multiply	RX	5C	M	189.90 + X_1 + 4.52C_{MR} + 4.52C_{MD} + 8.14C_{RE} − 36.18nz + 2.26N_B	+ 0.90DD
Multiply halfword	RX	4C	MH	113.55 + X_1 + 4.52C_{MR} + 4.52C_{MD} + 4.07C_{RE} − 36.18nz + 2.26N_B	+ 0.45DD
Multiply decimal	SS	FC	MP	56.53 − T + 5.43N_1 + 36.18N_2 + 9.50NMD 93.61 − T + 5.43N_1 + 69.61N_2 + 18.54NMD	
Multiply (long)	RR	2C	MDR	409.08 − 51.55nz + 3.62N_B	
Multiply (long)	RX	6C	MD	414.13 − 51.55nz + 3.62N_B	+ 1.80DD
Multiply (short)	RR	3C	MER	134.67 − 34.82nz + 1.81N_B	
Multiply (short)	RX	7C	ME	139.93 − 34.82nz + 1.81N_B	
OR	RR	16	OR	7.23 + 1.35CC0	
OR	RX	56	O	12.66 + X_1 + 1.35CC0	+ 0.90DD
OR	SI	96	OI	10.85 − S_1	
OR	SS	D6	OC	24.40 − T + 4.52N	
Pack	SS	F2	PACK	26.22 − T + 2.70N_1 + 1.80N_2	
Purge translation-lookaside buffer	SI	B20D	PTLB	10.85 − S_2 29.62 − S_2	
Reset reference bit	SI	B213	RRB	14.92 − S_2	

Instruction	Format	Op Code	Mnemonic	Average Time in Microseconds	Notes
Set clock	SI	B204	SCK	57.29 – S	
Set clock comparator	SI	B206	SCKC	83.30 – S	
Set CPU timer	SI	B208	SCT	32.57	
Set program mask	RR	04	SPM	9.04	
Set storage key	RR	08	SSK	16.73	
Set system mask	SI	80	SSM	55.74 – S (BC)	
				67.52 – S (EC without DAT)	
				82.89 – S (EC with DAT)	
Shift and round decimal	SS	F0	SRP	56.54; 215.53	
				96.30; 363.47	
Shift left double	RS	8F	SLDA	19.45 (minimum) 54.72 (maximum)	
Shift left double logical	RS	8E	SLDL	12.20 (minimum) 39.79 (maximum)	
Shift left single	RS	8B	SLA	15.37 (minimum) 37.99 (maximum)	
Shift left single logical	RS	89	SLL	9.94 (minimum) 25.32 (maximum)	
Shift right double	RS	8E	SRDA	17.63 (minimum) 45.21 (maximum)	
Shift right double logical	RS	8C	SRDL	13.11 (minimum) 39.34 (maximum)	
Shift right single	RS	8A	SRA	13.56 (minimum) 28.93 (maximum)	
Shift right single logical	RS	88	SRL	10.84 (minimum) 24.86 (maximum)	
Start I/O	SI	9C	SIO	65.41 – S_2	
				52.00 – S_2 + R_T	
Store	RX	50	ST	11.76 + X_1	+ 1.80ODD
Store character	RX	42	STC	10.40 + X_1	
Store and AND system mask	SI	AC	STNSM	63.00 – S_1	
				76.14 – S_1	
				87.45 – S_1	
Store and OR system mask	SI	AD	STOSM	62.55 – S_1	
				78.85 – S_1	
				87.00 – S_1	
Store clock comparator	SI	B207	STCKC	23.51 – S_2	+ 3.62ODD
Store CPU timer	SI	B209	STPT	32.13 – S_2	+ 3.62ODD
Store channel ID	SI	B203	STIDC	20.80 – S_2	
Store character under mask	RS	BE	STCM	10.10 – S_1 + 0.90nm3	
Store clock	SI	B205	STCK	30.30 – S_1	+ 3.62ODD
Store control	RS	B6	STCTL	14.47 – S_2 + 5.88R	
Store CPU ID	SI	B202	STIDP	19.44 – S_2	
Store halfword	RX	40	STH	9.95 + X_1	+ 0.90DD
Store (long)	RX	60	STD	21.70 + X_1	+ 3.60DD
Store multiple	RS	90	STM	9.50 – S_1 + 3.17R	+ R x 1.80ODD
Store (short)	RX	70	STE	16.74 + X_1	+ 1.80ODD
Subtract	RR	1B	SR	11.30 – 0.45CC0 + 0.90CC3	
Subtract	RX	5B	S	16.28 – 0.45CC0 + 0.90CC3	+ 0.90ODD
Subtract decimal	SS	FB	SP	81.83 + 5.43N_1 + 3.17N_2 – T	
				85.92 + 5.43N_1	
				+ 3.17N_2 + RC x 2.26N_1	
Subtract halfword	RX	4B	SH	15.37 + X_1 0.45CC0 + 0.45CC3	+ 0.45ODD
Subtract logical	RR	1F	SLR	11.31	
Subtract normalized (long)	RR	2B	SDR	57.93	
Subtract normalized (long)	RX	6B	SD	65.30 + X_1	+ 1.80DD
Subtract logical	RX	5F	SL	14.92 + X_1	+ 0.90DD
Subtract normalized (short)	RR	3B	SER	46.94	
Subtract normalized (short)	RX	7B	SE	52.21 + X_1	+ 0.90DD
Subtract unnormalized (long)	RR	2F	SWR	58.41	
Subtract unnormalized (long)	RX	6F	SW	63.58 + X_1	+ 1.80DD
Subtract unnormalized (short)	RR	3F	SUR	36.18	
Subtract unnormalized (short)	RX	7F	SU	50.41 + X_1	+ 0.90DD
Supervisor call	RR	0A	SVC	86.44	
				92.83	
				106.40	
Test and set	SI	93	TS	10.85 + X_1 – 0.45CC0	
Test channel	SI	9F	TCH	24.82 – S_2	
				38.90 – S_2 + RT	

Instruction	Format	Op Code	Mnemonic	Average Time in Microseconds	Notes
Test I/O	SI	9D	TIO	$35.73 - S_2 + RT$ $38.44 - S_2$	
Test under mask	SI	91	TM	$11.45 - S_1 - 0.90CC0$	
Translate	SS	DC	TR	$23.06 - T + 8.14N$	
Translate and test	SS	DD	TRT	$21.71 - T + 7.24N + 4.97U$	
Unpack	SS	F3	UNPK	$29.39 - T + 2.71N_1$	
Zero and add	SS	F8	ZAP	$62.86 - T + 2.26N_1 + 2.71N_2$	

ABBREVIATIONS

ACK	Acknowledgement (positive)
ACU	Automatic calling unit
ALU	Arithmetic and logic unit
ASCII	American National Standard Code for Information Interchange
BC	Basic control
BCC	Block check character
BCD	Binary-coded decimal
BKWD	Backward
bpi	Bits per inch
BSC	Binary synchronous communication
CAW	Channel address word
CCITT	Comité Consultatif International Téléphonique et Télégraphique
CCW	Channel command word
CD	Chained data
CE	Customer engineer
CPU	Central processing unit
CSW	Channel status word
DAT	Dynamic address translation
DIL	Do interpretive loop
DL	Data length
DLE	Data link escape
DOS	Disk operating system
EBCDIC	Extended binary-coded decimal-interchange code
EC	Extended control
EIB	Error index byte
ENQ	Enquiry
EOA	End of address
EOB	End of block
EOM	End of message
EON	End of number
EOT	End of tape
EOT	End of transmission
ERP	Error recovery procedure
ETB	End of text block
ETX	End of text
Hex	Hexadecimal
ICA	Integrated Communications Adapter
ID	Identity
IDAL	Indirect data address list
IDAW	Indirect data address word
ILT	In-line test
IMPL	Initial microprogram load
in.	Inch
I/O	Input/output
IOP	Input/output processor
IPL	Initial program load
ITB	Intermediate text block
KL	Key length
LF	Line feed
LRC	Longitudinal redundancy check
MFCM	Multi-function Card Machine
MFCU	Multi-function Card Unit
MIP	Machine instruction processor
mm	Millimeter
ms	Millisecond
MSC	Main storage controller
NAK	Negative acknowledgement
NL	New line
NPRO	Non-process run-out
NRZI	Non-return-to-zero inverted
ns	Nanosecond
OLSEP	On-line stand-alone executive program
OLT	On-line test
OMR	Optical mark read
Op	Operation
PCI	Program-controlled interruption
PE	Phase encoded
PER	Program event recording
PSW	Program status word
PTTC	Paper tape transmission code
RCE	Read column eliminate
RPQ	Request for price quotation
RPS	Rotational position sensing
RVI	Reverse interruption
SC	Solar cell
SLI	Suppress length indication
SOH	Start of heading
STX	Start of text
SVP	Service processor
SYN	Synchronization
TIC	Transfer in channel
TLB	Translation lookaside buffer
TOD	Time-of-day
TU	Tape unit

UCW	Unit control word
UCS	Universal character set
μs	Microsecond
VRC	Vertical redundancy check
WABT	Wait before transmit

GLOSSARY

Address Translation: The process of changing the address of an item of data or an instruction from its virtual address to its real storage address. See also *dynamic address translation.*

Basic Control (BC) Mode: A mode in which the features of a System/360 computing system and some additional System/370 features, such as new machine instructions, are operational on a System/370 computing system. See also *extended control (EC) mode.*

Bootstrap Program: A small microprogram in the service processor which starts the SVP to the point where it can load its own *main* microprogram from the console file.

Burst Mode: An operating mode in which the operation of a high-speed I/O device excludes all other I/O operations on a given input/output processor.

Control Registers: A set of registers used for operating system control of relocation, priority interruption, program event recording, error recovery, and masking operations.

Control Station: The station (usually a CPU) in a multipoint data communications system that controls network traffic by means of polling and selection. On a centralized multipoint network, tributary stations can communicate *only* with the control station, when polled or selected by the control station.

Control Storage: An area in a subprocessor where the microprogram is stored.

Cursor: A movable marker on the Model 115's video display, used to indicate the position of the next character to be entered on the screen.

Dynamic Address Translation: (1) The change of a virtual storage address to a real storage address during execution of an instruction. See also *address translation.* (2) A hardware feature that performs the translation.

Extended Control (EC) Mode: A mode in which all the features of a System/370 computing system, including dynamic address translation, are operational. See also *basic control (BC) mode.*

Front End: Electronic circuitry which connects an I/O device or a control unit to an input/output processor.

Hexadecimal: A number system that uses the equivalent of decimal number 16 as a base.

Input/Output Interface: The interconnection between I/O channels and different types of I/O devices.

Input/Output Processor: A subprocessor which, after initiation by the instruction processing unit, exerts complete control over I/O devices by means of its circuitry and microprogram logic, and operates in fully overlapping mode with the instruction processing unit and other input/output processors.

Integrated Adapter (or Attachment): A device which allows I/O devices to be attached to the system without a standard input/output interface.

Machine Instruction Processor (MIP): The MIP is a subprocessor of the Model 115 which carries out the instruction processing, selects input/output processors and handles interruptions. The MIP also incorporates the direct disk attachment.

Main Storage Controller: A subprocessor which controls all traffic to and from main storage, and keeps and updates the address registers.

Microinstruction: A basic or elementary machine instruction. Each program, each channel routine, and so on, consists of sequences of microinstructions.

Microprogram: A sequence of microinstructions, also termed a *microroutine.*

Modem: Contraction of *modulator/demodulator.* A device that converts digital dc signals into frequency-encoded signals to allow transmission over telephone lines. It also reconverts frequency-encoded signals received from a remote station into digital dc signals. In some countries, the term is applied to devices that have the functions of a data set and is considered synonymous with *data set.*

Momentary Key: A key which causes only one character entry per key depression regardless of how long the key is held down.

Multiplex: To interleave or simultaneously transmit two or more messages on a single channel.

Multipoint Network: A line or circuit that interconnects several stations in a data communications system.

Page: A fixed-length block of instructions, data, or both, that can be transferred between real storage and external page storage.

Page Table: A table that indicates whether or not a page is in real storage and correlates virtual addresses with real storage addresses.

Page Translation Exception: A program interruption that occurs when a virtual address cannot be translated by the hardware because the invalid bit in the page table entry for that address is set. See also *segment translation exception.*

Program Event Recording (PER): A hardware feature used to assist in debugging programs by detecting program events.

Real Address: The address of a location in real storage.

Real Storage: The storage of a System/370 computing system from which the central processing unit can directly obtain instructions and data, and to which it can directly return results.

Segment: A continuous area of virtual storage, which is allocated to a job or system task.

Segment Table: A table used in dynamic address translation to control user access to virtual storage segments. Each entry indicates the length, location, and availability of a corresponding page table.

Segment Translation Exception: A program interruption that occurs when a virtual address cannot be translated by the hardware because the invalid bit in the segment table entry for that address is set. See also *page translation exception.*

Service Processor: A subprocessor which loads programs, initializes the system, monitors for and logs errors, and handles the manual control of the system.

Subprocessor: One of a number of independent Model 115 control processors, which have their own clocking devices, storages, and controls, and which execute specific tasks such as processing instructions or servicing I/O devices. The subprocessors minimize interference between control and I/O operations in the system. The subprocessors are the main storage controller, the machine instruction processor, the service processor, and the input/output processors.

Tag Line: Defines the nature of information being transmitted over a bus.

Tributary Station: In a centralized multipoint data communications system, a station, other than the control station, that can communicate only with the control station when polled or selected by the control station.

Typamatic Key: A key that causes a single character entry when briefly depressed, and repetitive character entry as long as it is held down.

Virtual Address: An address which refers to virtual storage and must, therefore, be translated into a real storage address when it is used.

Virtual Storage: Addressable space that appears to the user as real storage, from which instructions and data are mapped into real storage locations. The size of virtual storage is limited by the addressing scheme of the computing system and by the amount of auxiliary storage available, rather than by the actual number of real storage locations.

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